Analysis of On-Chip Interconnects using Prospective Neural Network Techniques

by

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Declaration

I hereby declare that

i) the thesis comprises of my original work towards the degree of Master of Technology in Information and Communication Technology at Dhirubhai Ambani Institute of Information and Communication Technology and has not been submitted elsewhere for a degree,

ii) due acknowledgment has been made in the text to all the reference material used.

Ajita Misra

Certificate

This is to certify that the thesis work entitled ANALYSIS OF ON-CHIP INTERCONNECTS USING PROSPECTIVE NEURAL NETWORK TECHNIQUES has been carried out by Ajita Misra for the degree of Master of Technology in Information and Communication Technology at *Dhirubhai Ambani Institute of Information and Communication Technology* under our supervision.

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Contents

Abstract

With the advancement in technology the number of transistors being fabricated on a single integrated chips (IC) increase manifold as stated in Moore's law. Due to this increase in the transistors and thereby shrinking of the devices one of the major problematic areas for designers are interconnects which are responsible for the connection of the devices with each other and to power supply and ground. Thus analysis of on-chip interconnect is a necessary for designing a circuit. The mathematical representation of interconnect using finite difference time domain (FDTD) methodology with CMOS receiver is proposed in this research. The model used for the purpose is a driver-interconnect-load (DIL) model. In order to analyze and further design interconnect circuits, neural network techniques has been employed. Levenberg-Marquardt (LM) algorithm is used for implementing back-propagation in neural network (NN) design. NN based models have been extensively explored for classification, pattern recognition applications, image-speech processing, system and control identification, medical diagnosis, finance, etc. However, this has been very limitedly explored and adopted for optimization, designing and performance evaluation of VLSI circuits and systems. The optimization and designing of billions of transistors is a time consuming task. The NN based model efficiently automates the complete process. The dataset for training the network has been created using HSPICE . The accuracy of the proposed NN based model is assessed using regression, mean square error and error histogram. Further graphene materials such as multilayer graphene nanoribbon (MLGNR) has been explored as an alternative material for the DIL system. Its application is also validated in ring oscillator thereby proving a superiority over the traditional materials for interconnect system

Keywords: *On-chip interconnects, neural network (NN), Finite difference time domain (FDTD), variabilty analysis, multilayer graphene nanoribbon (MLGNR) .*

List of Symbols and Acronyms

$ANOVA$ Analysis of variance

BP Back-propagation

CFL Courant- Friedrichs-Lewy

$CMOS$ Complementary metal oxide semiconductor

DIL Driver-interconnect-load

ESC Equivalent single conductor

$FDTD$ Finite difference time-domain

FET Field-effect transistor

$HSPICE$ Hewlett Simulation Program with Integrated Circuit Emphasis

IC Integrated circuits

LM Levenberg–Marquardt

MC Monte Carlo

$MLGNR$ Multilayer graphene nanoribbon

MSE Mean square error

MTL Multi-conductor transmission line

$NMOS$ N-type metal-oxide-semiconductor

NN Neural Network

PC polynomial chaos

PCB printed circuit board

PDP Power delay product

$PMOS$ P-type metal-oxide-semiconductor

R Regression coefficient

SVR Support vector regression

TEM Transverse electric and magnetic

$US-FDTD$ Unconditionally stable finite difference time-domain

$VLSI$ Very large scale integration

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Chapter 1
Introduction

Moore's law states that number of transistors being fabricated in integrated circuits (IC) increases nearly two times in every two years. Due to this scaling down of technology interconnects become a major bottleneck for IC designers. Since number of transistors increase the IC becomes densely packed and therefore various signal integrity issues crop up. Also variability can be induced in interconnects due to manufacturing process which result in uncertain parameters. Due to these issues the analysis of on-chip interconnects is a major issue.

The conducting materials used to connect different modules, provide power supply and ground to a circuit are known as interconnects. These are stacked on top of each other in orthogonal position. The thickness of these interconnects increase as we move from bottom to top layer. Further, they are classified into three types namely- local, semi-global and global based on their structure and which circuit elements they connect. Local interconnects constitute the bottom layer being usually first and second metal layer. These are short thin wires connects few gates or transistors within a module or functional block. The next few layers are the intermediate or semi-global interconnects which are longer and wider compared to local interconnects and therefore provide less resistance. Intermediate interconnects provide signal or clock distribution within a block and are typically around 3 mm in length. Global interconnects occupy the top layers of interconnects and usually more than 4 mm in length. These interconnects provide signal or clock distribution to the entire circuit and connect different modules. Earlier Aluminum was used as an interconnect material but later it was replaced by copper which is still prevalent today's chips. Graphene has emerged as one of the promising prospective material which can be used to replace copper for better functionality of the system. Therefore in this research the effect of graphene as a potential interconnect material will also be considered for analysis.

Neural networks (NN) mimic the biological functioning of a human brain thereby learning from different processes and further applying them in different

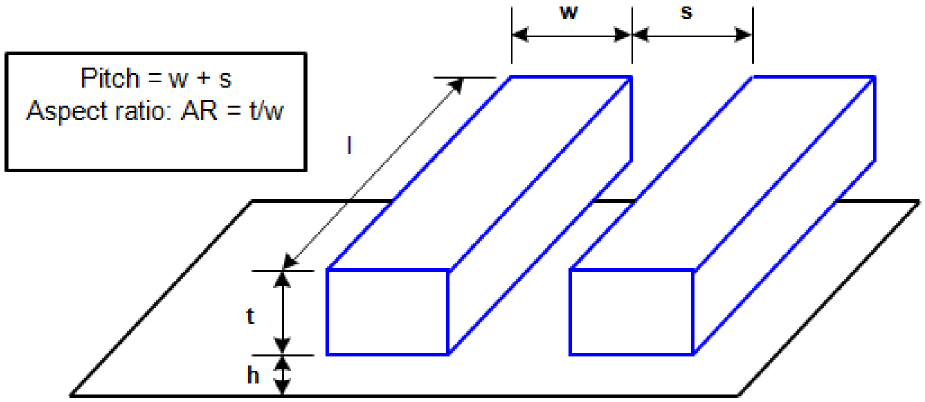

Figure 1.1: Interconnect structure

scenario. NN structure consists of neurons which are connected to each other with different strength which are defined as weights. These weights are readjusted in training process to give minimum mean square error (MSE) with is considered as a performance parameter of NN. The readjustment is done using back propagation algorithm. There are various back propagation algorithms such as gradient descent, quasi-newton, Levenberg–Marquardt (LM) etc. Based on the speed and memory needed for a particular problem the optimum algorithm is selected. Due to the NN technique the multiple iterations used in traditional analysis method is replaced by only a one- time training process thereby increasing the efficiency of the system. The research aims to bridge the gap between VLSI and machine learning by proposing a surrogate model for analysis and design of interconnect system.

1.1 On-Chip Interconnect

Electrical modeling is used for interconnect modeling where resistance, inductance and capacitance are the parasitics. The interconnect structure can be observed in Figure 1.2.

The parasitics of a wire viz. resistance and capacitance in general are distributed along its length and are not lumped into a single position. However, at low frequencies and short wire lengths, only capacitive and resistive components of the wire can be considered. The distributed capacitance and resistance of the wire can be lumped into a single capacitor and resistor. Distributed RC model is more appropriate and accurate than lumped model. For long interconnects, when the physical dimensions of interconnect are in the range of the wavelength of the

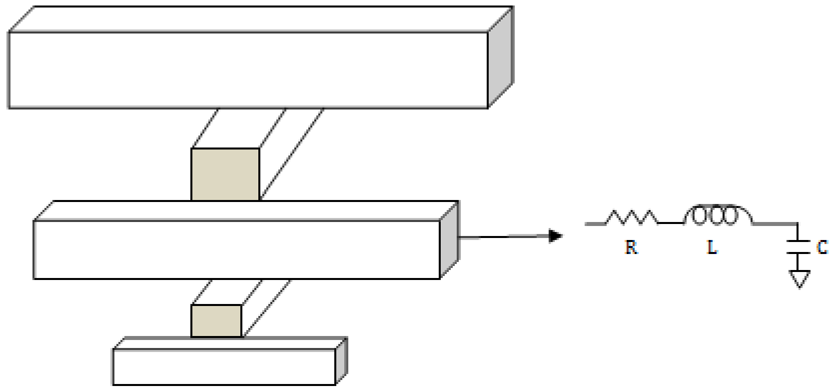

Figure 1.2: Interconnect equivalent electrical model

signal passing through the interconnect, lump model become inefficient. Henceforth, distributed model is used. The transmission line has the prime property that signals propagate over the interconnection medium as wave which is not the case in distributed RC model. The signal propagates by alternatively transferring energy from the electric to the magnetic fields, or equivalently from the capacitive to the inductive modes

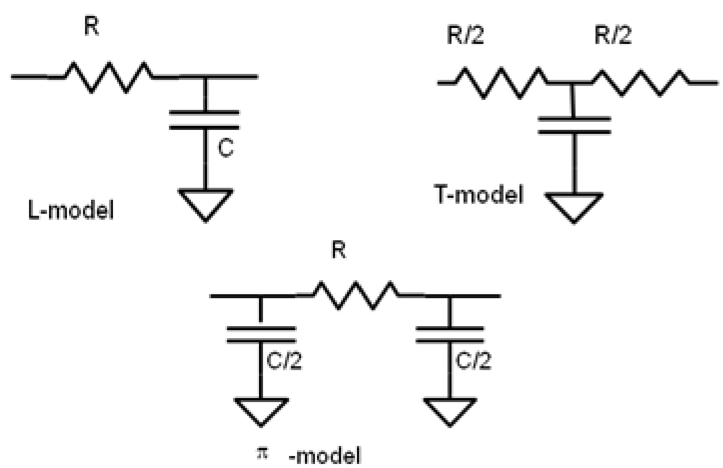

Figure 1.3: L, T and pi equivalent electrical model

The term MTL stands for multi-conductor transmission line that means a set of parallel conductors are used to transmit electrical signals between source and load. The dominant mode of propagation is transverse electric and magnetic (TEM) mode in MTL. the MTL model is solved to a equivalent simplified model. This is known as equivalent single conductor (ESC) model.

In order to analyze the performance of interconnects FDTD is one of the widely used model which has been used in this research. Further the outputs are enhanced using US-FDTD technique. Also variability analysis has been done using Monte Carlo simulations in which the parameters are varied simultaneously in order to get their cumulative effect on the circuit performance. Although these methods are widely established yet they have high computational cost especially while dealing with circuits with large number of connections. Therefore a new method is proposed for on-chip interconnect analysis using neural network which curbs the computational cost.

1.2 Neural Network

Machine learning is a study of algorithms that improves the performance at some task with experience. The learnt regression model can keep learning new entry data and the model prediction becomes more and more precise. It has been employed in various fields such as -Natural language processing, Speech recognition, Computer vision, Robot control. Machine Learning can be classified into three categories namely supervised, unsupervised and reinforcement learning. Regression is class of supervised learning. It is a task of predicting the value of target (numerical variable) by building a model based on one or more predictors (numerical and categorical variables). The benefits of regression analysis are:

1. It indicates the significant relationships between dependent variable and independent variable.
2. It indicates the strength of impact of multiple independent variables on a dependent variable.

Neural Network is a class of regression algorithm

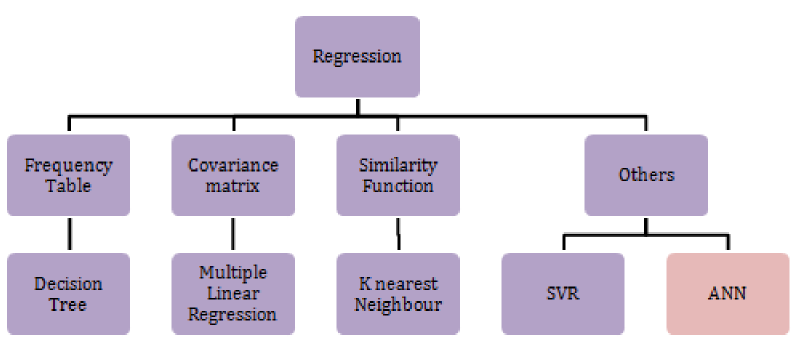

Figure 1.4: Types of Regression algorithm

Neural networks (NN) mimic the biological functioning of a human brain thereby learning from different processes and further applying them in different scenario. This can be seen in Fig. 1.5

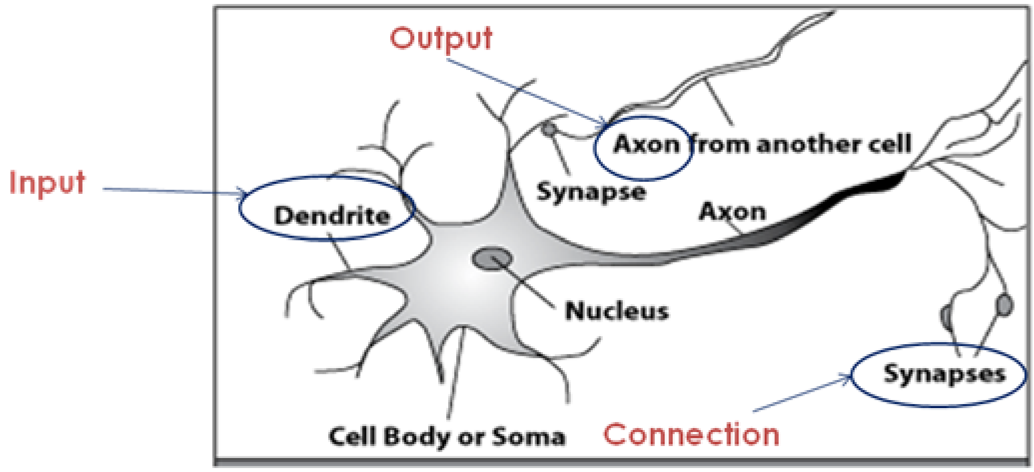

Figure 1.5: Correlation of neuron in brain to neural network

NN structure consists of neurons which are connected to each other with different strength which are defined as weights. These weights are readjusted in training process to give minimum mean square error (MSE) with is considered as a performance parameter of NN. The readjustment is done using back propagation algorithm. There are various back propagation algorithms such as gradient descent, quasi-newton, Levenberg–Marquardt (LM) etc. Based on the speed and memory needed for a particular problem the optimum algorithm is selected. Due to the NN technique the multiple iterations used in traditional analysis method is replaced by only a one- time training process thereby increasing the efficiency of the system.

The research aims to bridge the gap between VLSI and machine learning by proposing a surrogate model for analysis and design of interconnect system. .

CHAPTER 2
Literature Review

Interconnects play a major role in overall functioning of the circuit. The analysis of on-chip interconnects has been reported in various research papers. Machine learning has been employed in various fields and it has been attempted to integrate it with electronic circuit design. These researches have been presented in this section along with their work and research gaps.

2.1 Interconnect analysis

Vobulapuram Ramesh Kumar, Brajesh Kumar Kaushik and Amalendu Patnaik [1] proposed finite difference time domain (FDTD) modelling for interconnects with non linear CMOS driver. In FDTD interconnect line is discretized in both space and time domain. In earlier research the CMOS driver is considered as a linear resistor but in this paper different regions of operation is considered and therefore a non-linear driver is used. It considers alpha power law model to represent transistors in CMOS driver. The voltage and current are determined at near end and far end terminal. [2] proposes FDTD for interconnects with non linear CMOS driver represented with n^{th} power law model. N^{th} power law model is advanced technique compared to alpha power law model as it considers the aspect ratio into account. In both [1] and [2] the load is modelled as an equivalent capacitor. Due to this assumption in load the static power dissipation is ignored at the output. Also only crosstalk analysis performed in the paper which can be further added with power dissipation, delay of interconnects etc.

Vobulapuram Ramesh Kumar, Arsalan Alam, Brajesh Kumar Kaushik and Amalendu Patnaik [3] proposes unconditionally stable finite difference time domain (US-FDTD) model to overcome Courant- Friedrichs-Lewy (CFL) stability condition. According to CFL condition maximum time step size is limited such that $\Delta t_{max} = \Delta z/v_{max}$. Although various US-FDTD methods have been proposed for modeling transmission lines having resistive driver and load but in VLSI it is essential to take the non- linearity into consideration. Thus this paper gives an approach to model using on-chip interconnects which are free from time step restriction. In order to model the interconnect line forward and backward difference approximation is used in space domain. Further to model CMOS driver modified alpha power law model is incorporated. It is observed that the given technique is more efficient than traditional FDTD method as it reduces the time taken in the process and also gives a stable output for any given time step.

Mayank Kumar Rai, Ashoke Kumar Chatterjee, Sankar Sarkar, and B. K. Kaushik [4] shows performance analysis in terms of delay, power and power delay product of multilayer graphene nanoribbbon (MLGNR) as an interconnect material. It is compared for different interconnect lengths with copper material. It can be seen that MLGNR performs better than copper for longer interconnects (>200 μ m). Also the effect of interlayer resistance is depicted for different lengths. It can be seen that smaller lengths have significant impact due to this resistance when compared with longer interconnects.

Girish Kumar Mekala, Yash Agrawal and Rajeevan Chandel [5] shows the performance analysis of dielectric inserted side contact graphene nanoribbon (Di-side-GNR) using US-FDTD technique. Comparison between the proposed model and conventional FDTD model for copper, Di-side-GNR and side- GNR have depicted in terms of output voltage, power dissipation and crosstalk in phase delay. Also CMOS and resistive driver are compared thereby showing that CMOS driver gives better accuracy. Although further analysis and comparison with conventional FDTD modeling can be done on the basis of delay and power delay product (PDP). This method can is done for two coupled lines but it can be extended for n coupled lines.

Agrawal, R. Chandel R. Dhiman [6] analysed the variability effects in interconnects caused during manufacturing process. Due to variation in parameters such as spacing (s), height (h), thickness (t) and width (w) the electrical parasitics of interconnects is affected. The variations in geometry of the interconnects can be due to the fluctuations induced in oxide thickness, effective length and threshold voltage. Methods such as process corner, parametric analysis, Monte Carlo, Taguchi and rank table analysis have been suggested for observing the effect of variability and its consequence in overall performance of the system. In process corner analyses driver – interconnect- load (DIL) model is used and the effect of fast, slow and typical PMOS and NMOS is considered. Parametric analysis considers the effect of each parameter variation on the circuit performance whereas Monte Carlo considers the cumulative effect on the output due to varying parameters. ANOVA and rank table analyses the factors affecting the system performance based on how strong or weak the influence is. This is done by providing different tables or rank to different varying parameters.

2.2 Machine Learning

A. Hafid Zaabab, Qi-Jun Zhang and Michel Nakhla [7] Presents neural network (NN) as microwave circuit optimisation technique for circuit or design level but the learning algorithm used is slow and focuses on local minima rather than global minima. It gives an idea about training sets and different training parameters to be used. Different circuits have been modeled using NN such as amplifier circuit, transmission line circuit and MESFET thereby depicting the generality of the NN model.

Riccardo Trinchero, Paolo Manfredi, Igor S. Stievano and Flavio G. Canavero [8] investigates the application of polynomial chaos (PC) , Support vector regression (SVR) for printed circuit board (PCB) interconnect modeling. Monte Carlo (MC) is used for dataset creation. Further the techniques are compared with the addition of noise and it can be observed that the performance of SVM performance is better than PC as it takes into account the non- linear relationship between input and output into account. Further the computational efficiency of neural network is confirmed as optimum results are obtained in much less number of samples.

M. I. A. Lourakis [9] presents Levenberg–Marquardt (LM) algorithm which is formed by combining steepest descent and the Gauss-Newton method. It can be employed to locate the minimum of the function. Since steepest descent is slow but converges correctly it is paired with Guass –Newton method to give a faster convergence.

P. Sibi, A Bordes , SA Jones, P Siddarth [10] presents an overview of different activation functions which are used to incorporate non linearity and transform the input to an output function. Activation function plays a key role in back propagation algorithm which is employed to minimize the error of neural network. Comparison between different functions is shown based on a common dataset thereby giving an idea about the selection of an appropriate function with respect to the problem statement.

CHAPTER 3

Research Objectives

As the scaling moves towards nanometer regime the output performance of VLSI system is severely affected due to interconnect performance. The demands of higher speed, higher operational frequency, lower power dissipation and smaller chip size have made on-chip interconnects very important research topic. The VLSI interconnect material i.e. copper (Cu) is facing various problems such as delay, power dissipation,electromigration, surface scattering and grain boundary scattering as the technology is scaled down. These problems are severe and degrade the performance of Cu interconnect. Due to these reasons there is dire need for an alternative material to Cu interconnects which can perform better than it. Graphene nanoribbons (GNRs) are the suggested alternatives to Cu as they offer high thermal conductivity and large current carrying capacity over copper interconnects. Also since the traditional analysis and designing methods are time consuming for large circuits, alternative method namely NN has been proposed. The objectives are detailed as follows

1. **Mathematical formulation using FDTD technique with practical CMOS driver and receiver**

   The analytical mathematical model is formulated using numerical method based FDTD technique. The methodology is extended for a proposed DIL model which utilises a practical CMOS driver and CMOS load. The MATLAB results are compared with the HSPICE simulation.

2. **Mathematical modeling using US-FDTD technique**

   The enhanced mathematical model is proposed using US-FDTD technique for DIL model with capacitive load.The analytical results are compared with the HSPICE simulation and FDTD model.

3. **Neural Network Based Performance Evaluation of On-Chip Interconnect System**

   The neural network model provides faster prediction when compared to the traditional performance analysis method. Also the proposed method works closely with the simulation methods thereby depicting the accuracy of the developed model. The dataset used for training of neural network (NN) is created using HSPICE. Performance parameters considered are delay and power dissipation. The several analyses are performed at 32nm technology.

4. **Neural Network Based Optimized Designing of On-Chip Interconnect System**

   Automated design methodology is created in order to optimize the aspect ratio of the driver for the on-chip interconnect system. This automation is performed by employing NN technique. The training and testing sets are created using HSPICE. After the validation of the network, the optimum aspect ratio is obtained by providing the desired performance attributes as input.The output performance parameters considered during optimized designing of the system are delay, power dissipation and loading effects.

5. **Variability Analysis of interconnects using machine learning techniques**

   Analyzing the impact of process variations on interconnect is essential for predicting the reliability of graphene based interconnects. Monte Carlo has been a widely used variability technique. Henceforth in this objective Monte Carlo analysis has been incorporated for creating initial dataset for on-chip neural network based model. NN replaces the manual time taking process used in traditional variability analysis method and speeds up the process of optimally designing of the system.

6. **Performance analysis of graphene interconnects with graphene MOSFET.**

   A novel DIL model consisting of MLGNR material for both interconnect and driving MOSFET has been proposed. This is compared in terms of performance with its silicon counterparts. Also its practicality is tested through a ring oscillator which shows better performance than the existing silicon material

CHAPTER 4

Mathematical modeling using FDTD technique

The performance of interconnects have been evaluated using various models in the past. Moment matching technique is method for performance evaluation using taylor series expansion [11]. The approximation using the first moment is utilised to form elmore delay model. It provides performance in terms of delay while considering interconnects as RC trees and therefore has a drawback of not considering the contribution of inductance in overall delay of the interconnect. Sakurai model [12] was developed to calculate delay using time response expression but it was also limited to RC lines. Ismail et al. [13] developed model using RLC circuit and showed that exclusion of inductance results in inaccurate prediction of delay. Although the driver in this case was considered as an RC element and it limits the modeling scheme. Another method for performance prediction is the two port method [14]. This method considers four ports where two are input ports and the other two are the output ports. The topology of the network between these ports defines the input-output relationship. Some of such methods are ABCD, g, h, y and z models. Beside these circuit evaluation methods numerical methods have also been employed for interconnect analysis. In this technique, instead of considering the circuit as a lumped or distributed model the model is considered as 2D or 3D which exhibit electromagnetic characteristics. One of such method is finite element method (FEM). In this technique the modeling is done using partial differential equations which are restricted due to certain boundary conditions. Also finite elements are created as the large segments are divided to smaller segments. One of the methods of FEM is finite difference time domain technique (FDTD) [15] [16]. In FDTD method the differential equations are converted to discrete form in both time and space domain using central difference approximation method [17].

Courant's condition to employed to define maximum time step size ($\Delta\ t_{max}$) which satisfies the condition $\Delta\ t_{max} \leq \Delta z\ /\ v_{max}$. Here v_{max} is the phase velocity and Δz is the step size in space domain. In this modeling scheme near and far end boundary conditions are defined. The near end boundary is defined using the MOSFET models such as nth power law for the driving non-linear CMOS. The far end boundary is defined based on the terminating load. Till date the load considered was resistive in nature and later replaced by capacitive load. The material used for interconnect applications is usually copper in the current scenario. Although due to the advancement of technology the potential of copper becomes limited. The output performance is affected due to issues such as electromigration effect [18], delay and power dissipation. These problems can be overcome by graphene which is an allotrope of carbon [19], [20]. Graphene interconnects are mainly divided into carbon nanotube (CNT) [21], [22] and graphene nanoribbon (GNR) [23], [24]. This research uses multilayer GNR (MLGNR) as an interconnect material since it has higher mean free path, it is resistant to electromigration effect and also its fabrication can be controlled as compared to CNTs [19].

4.1 Model Formulation of DIL System using FDTD Technique

Numerical method based FDTD technique has been fore mostly utilized in the fields and applications of electro-magnetic by solving the Maxwell's equations [9], [25], [26]. This technique usually involves computations in both time and space domains. The FDTD technique is executed in leapfrog stepping manner with electrical (E) and magnetic (H) fields as its parameters [9], [27]. Later this method has been prospectively employed for performance characterization of on-chip interconnect system with voltage (V) and current (I) being analogous to E and H. Conventionally, modelling of driver and load were performed in time domain while interconnect were modelled in frequency domain. These cause time to frequency or reverse conversion problem. To mitigate this issue, FDTD model has been found appropriate. The conditions to be met during FDTD modelling are as follows [28]

1. The spatial step size (Δz) should be smaller than the wavelength (usually 10-20 times smaller than the wavelength).

2. The time step size (Δt) should satisfy the Courant's condition.

The voltage and current along interconnect can be defined by Telegrapher's equations as:

$$\frac{\partial v(x,t)}{\partial x} = -Ri(x,t) + L\frac{\partial i(x,t)}{\partial t} \tag{4.1}$$

$$\frac{\partial i(x,t)}{\partial x} = -C\frac{\partial v(x,t)}{\partial t} \tag{4.2}$$

Here v and i are the voltage and current variables of the on-chip interconnect whereas R, L and C are the parasitics namely resistance, inductance and capacitor respectively. Based on (4.1) and (4.2), the voltage and current at any specific point along the length of interconnect and particular instant of time can be derived using FDTD formulations. The interconnect of length l can be divided into Nx segments where Nx = l / Δz. This results in:

$$i_k^{n+1.5} = B.D.i_k^{n+0.5} + B(v_k^{n+1} - v_k^{n-1}) \tag{4.3}$$

$$Where, B = [\frac{\Delta x}{\Delta t}.L + \frac{\Delta x}{2}.R]^{-1} \tag{4.4}$$

$$AndD = [\frac{\Delta x}{\Delta t}.L - \frac{\Delta x}{2}.R] \tag{4.5}$$

$$v_k^{n+1} = v_k^n + A(i_{k-1}^{n+0.5} - i_k^{n+0.5}) \tag{4.6}$$

where, k = 2, 3, .., Nx

$$andA = \frac{\Delta x}{\Delta t}.C \tag{4.7}$$

After defining the general V and I for interconnect it is necessary to define the boundary conditions for the driving CMOS transistor and terminating load of the DIL system

Near-end boundary condition- k is kept as 1 and Δ z is replaced by Δ z/2, thereby using equation (4.6) the results obtained are:

$$v_1^{n+1} = v_1^n + 2A(i_{00}^{n+0.5} - i_1^{n+0.5}) \tag{4.8}$$

$$v_1^{n+1} = v_1^n + 2A(\frac{i_{00}^{n+1} + i_0^n}{2} - i_1^{n+0.5}) \tag{4.9}$$

Here i_{00} is the current of the driving transistor which is obtained by using Kirchoff's current law

$$i_{00} = C_m[\frac{\partial(v_s - v_1)}{\partial(t)}] + i_p - i_n - C_d.\frac{\partial v_1}{\partial t} \tag{4.10}$$

where C_m and C_d are the drain to gate coupling capacitance and drain diffusion capacitance of driving inverter respectively. i_p is the current of PMOS and i_n is the current of NMOS. i_n and i_p are derived using the nth power law [29].

Far-end boundary condition with capacitive load - k is kept as Nx+1 and Δ z is replaced by Δz/2, thereby using equation (4.6) the results obtained are:

$$v_{Nx+1}^{n+1} = v_{Nx+1}^{n} + 2A(i_{Nx}^{n+0.5} - \frac{i_{Nx+1}^{n+1} + i_{Nx+1}^{n}}{2}) \tag{4.11}$$

$$i_{Nx+1} = C_L[\frac{\partial(v_{Nx+1})}{\partial(t)}] \tag{4.12}$$

$$v_{Nx+1}^{n+1} = v_{Nx+1}^{n} + 2AF(i_{Nx}^{n+0.5} - \frac{i_{Nx+1}^{n}}{2}) \tag{4.13}$$

$$Where, F = [U + AC_L/\Delta t]^{-1} \tag{4.14}$$

Proposed model - For a driver interconnect load model terminated by an active gate load i.e. capacitor, a trade-off exists between short circuit and dynamic power dissipation in on-chip interconnects. Therefore, FDTD model with CMOS load has been proposed. To implement this, the far end boundary condition of the conventional FDTD model for VLSI interconnects has been replaced by utilizing nth power law model. This can be defined as:

$$v_{Nx+1}^{n+1} = v_{Nx+1}^{n} + 2A(i_{01}^{n+0.5} - i_{Nx+1}^{n+0.5}) \tag{4.15}$$

$$v_{Nx+1}^{n+1} = v_{Nx+1}^{n} + 2AF(\frac{i_{01}^{n+1} + i_{01}^{n}}{2} - i_{Nx+1}^{n+0.5}) \tag{4.16}$$

Here i_{01} is the current of the load CMOS transistor which is obtained by using Kirchoff's current law

$$i_{01} = C_m[\frac{\partial(v_{Nx} - v_{Nx+1})}{\partial(t)}] + i_p - i_n - C_d.\frac{\partial v_{Nx+1}}{\partial t} \tag{4.17}$$

where C_m and C_d are the drain to gate coupling capacitance and drain diffusion capacitance of driving inverter respectively. i_p is the current of PMOS and i_n is the current of NMOS. i_n and i_p are derived using the nth power law [29]. The current values depend on different regions of operation namely linear, saturation and cut-off regions [29] [30]. The detailed process flow for implementation of FDTD model is depicted in Fig. 4.1. The first step is the electrical parasitic description corresponding to the geometry of the considered interconnect. Thereafter, voltage and current variables are initialized based on the starting input condition. Next step is the iterative evaluation of voltage and current at particular distance points along interconnect length and time intervals. These include incorporation and coherence with the near- and far-end boundary conditions. This process is iteratively executed till maximum defined time and length is attained.

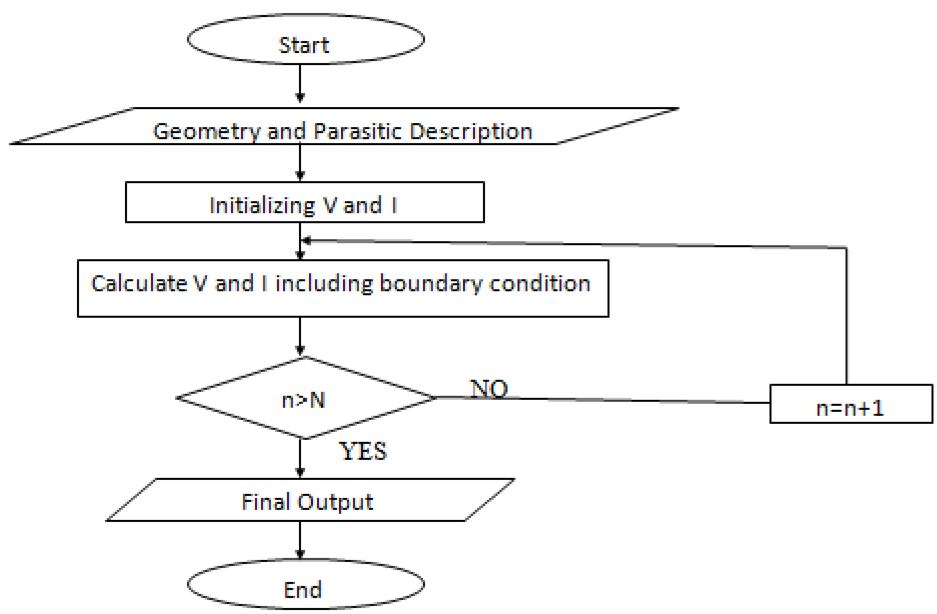

Figure 4.1: Flow diagram representing procedural execution steps for FDTD model implementation

4.2 Results and discussion

The output analysis of side contact MLGNR has been performed using FDTD and compared with the simulation results. Performance between copper and MLGNR is compared with delay and power dissipation as the output parameters. Further analysis of interconnect with CMOS load has been observed using the proposed methodology. The input parameters for MLGNR which are the electrical parasitics of the interconnect namely resistance (r), inductance (l) and conductance (c) have been taken from [31] whereas the parasitics for copper have been taken from [32] [33].The technology used for the analysis is 22nm. The aspect ratio considered for CMOS transistor is 2:1 and the capacitive load is taken as 2fF. The input given is a falling ramp signal from 0.9V to 0V.

4.2.1 Performance comparision between copper and graphene interconnects

The performance evaluation of copper and MLGNR has been compared in this section. The performance parameters are taken as delay and power dissipation. The length of interconnect are varied from 0.5mm to 3mm. Further the analysis has been done using SPICE and FDTD methods are compared. It can observed that the results obtained using FDTD are comparable to the SPICE modeling. The error percentage between the mathematical model and simulation result is approximately 1 percent. The delay curve is plotted in Fig.4.2. and it can be observed that the MLGNR gives much less delay when compared to copper interconnect. Also with increase in length the delay also increases therefore interconnect length is directly proportional to delay. Fig. 4.3. depicts the power dissipated by the interconnect with respect to its length. Here it can be seen that the dissipation increases as the interconnect becomes longer.

Further it can be observed that power dissipated by graphene interconnect is much less than that of copper interconnect. Therefore graphene is a suitable alternative for on chip interconnect as it gives better performance compared to the commonly used interconnect material in today's modern technology. Since global interconnects are longer and therefore MLGNR can be used.

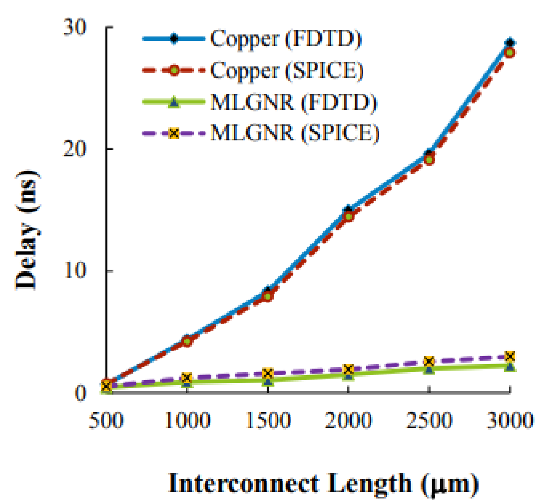

Figure 4.2: Delay in copper and MLGNR

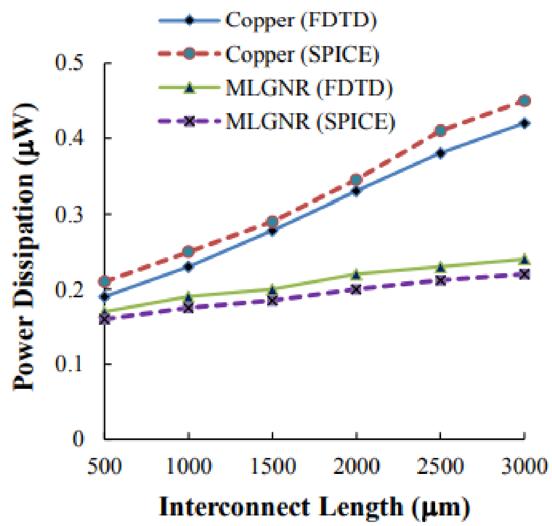

Figure 4.3: Power dissipation in copper and MLGNR

4.2.2 Assessment efficiency and robustness of the proposed FDTD based technique

In this section,the performance of DIL system is assessed using proposed FDTD and conventional FDTD models. The proposed model incorporates the practical CMOS inverter as load while in the conventional FDTD model, CMOS inverter has been approximated as capacitive load. The proposed model is also validated with SPICE simulation results. For model assessment, transient analysis has been implemented. The interconnect length is taken as 1mm. Thus using a transistor load provides as closer outlook to the real time application. The transient analysis has been shown in Fig. 4.4. where the simulation and mathematical modeling techniques are compared. It has been observed that mean error of 1 percent exists between the SPICE simulation and FDTD model with capacitive load whereas mean error is 1.8 percent between the SPICE simulation and the proposed method using CMOS load

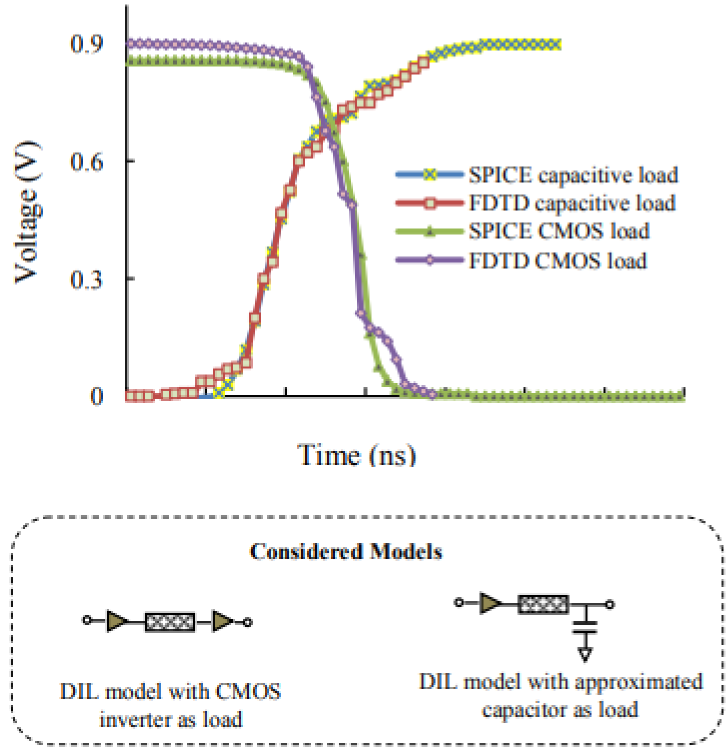

Figure 4.4: Comparision of output of DIL model with capacitive and CMOS load

Chapter 5

Mathematical modeling using US-FDTD technique

The FDTD methodology has been widely employed for electromagnetic problems and then have been further explores in the VLSI domain. This involves discritisation in space and time domain and is restricted to CFL stability condition as shown in chapter 4. Since the interconnects in the present scenario are longer, conventional FDTD techniques consume large memory space and power due to the enormous number of iterations required for the analysis. Hence, beyond the CFL condition, the FDTD technique is unstable and within it, the technique is not efficient. The improvements in FDTD technique can be easily addressed if the CFL stability condition is removed. Recently, several researchers have proposed various modified FDTD techniques to overcome the CFL stability criteria based on different algorithms, such as alternating direction implicit (ADI)-FDTD [34] [35], split-step FDTD [36] [37], Crank-Nicolson (CN)-FDTD [38] [39] and others [40] [41] [42]. All these techniques were developed for transmission lines that are usually excited and terminated by resistive drivers and resistive loads, respectively. However, the VLSI interconnects are driven and terminated by the nonlinear CMOS drivers and capacitive loads, respectively. Therefore, the existing unconditionally stable FDTD techniques are not suitable to analyze the performance of CMOS gate driven VLSI interconnects. In USFDTD technique, stability issue of FDTD technique has been mitigated by discretising voltage and current solutions staggered only in space. This eliminates Courant condition, by allowing a large time step size as compared to FDTD.

5.1 Model formulation using US-FDTD

This section involves development of US-FDTD model with a CMOS driver and capacitive load as termination for interconnect lines. The DIL model used for model formulation is depicted in figure 5.1.The total interconnect length is divided into Nz number of sections, each with a uniform length of Δz.

Telegrapher's equation 4.1 and 4.2 is used and forward difference approximation and backward difference approximation in space domain are applied. This results in

$$v_{k+1} - v_k + r.\Delta z.i_k + l.\Delta z.\frac{\delta i_k}{\delta t} = 0 \tag{5.1}$$

$$\frac{i_k - i_{k-1}}{\Delta z} = -c\frac{\delta v_k}{\delta t} \tag{5.2}$$

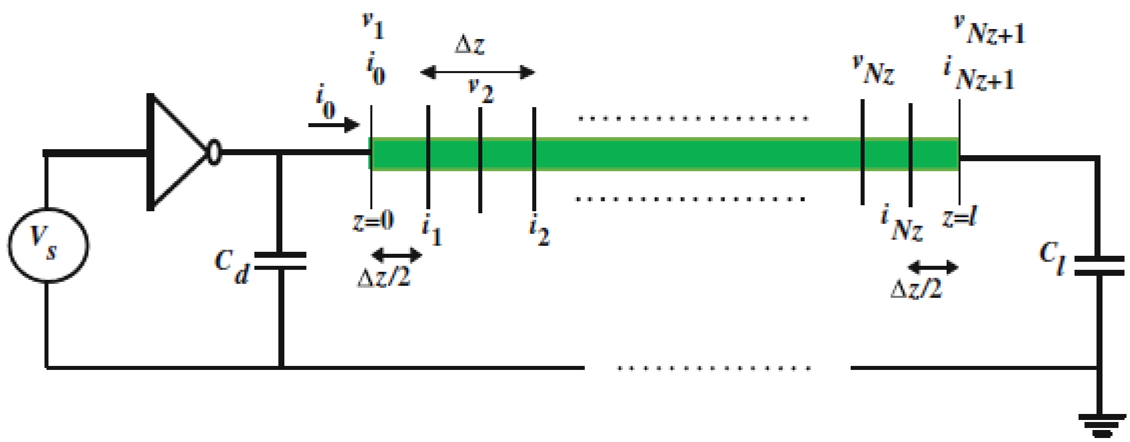

Figure 5.1: Representation of space discretization of an interconnect line for US-FDTD technique

For k = 2, 3, . . . , Nz, Eq. (5.2) results in

$$i_k - i_{k-1} + c\Delta z.\frac{\delta v_k}{\delta t} = 0 \tag{5.3}$$

For k=1 and k=Nz+1 the space segment is replaced by $\Delta z_{\overline{2}}$. This results in:
For k=1

$$i_1 - i_0 + \frac{c\Delta z}{2}.\frac{\delta v_1}{\delta t} = 0 \tag{5.4}$$

For k= Nz+1

$$i_{Nz+1} - i_{Nz} + \frac{c\Delta z}{2}.\frac{\delta v_{Nz+1}}{\delta t} = 0 \tag{5.5}$$

Equation 5.3, 5.4 and 5.5 have been further modified based on boundary condition. The detailed equation can be referred from [31]

The CMOS driver has been modelled using modified alpha law since it takes into account the short channel effects namely velocity saturation effect along with the finite drain conductance parameter which are not considered in the case of alpha power law model.

Detailed flowchart has been depicted in Fig.5.2.

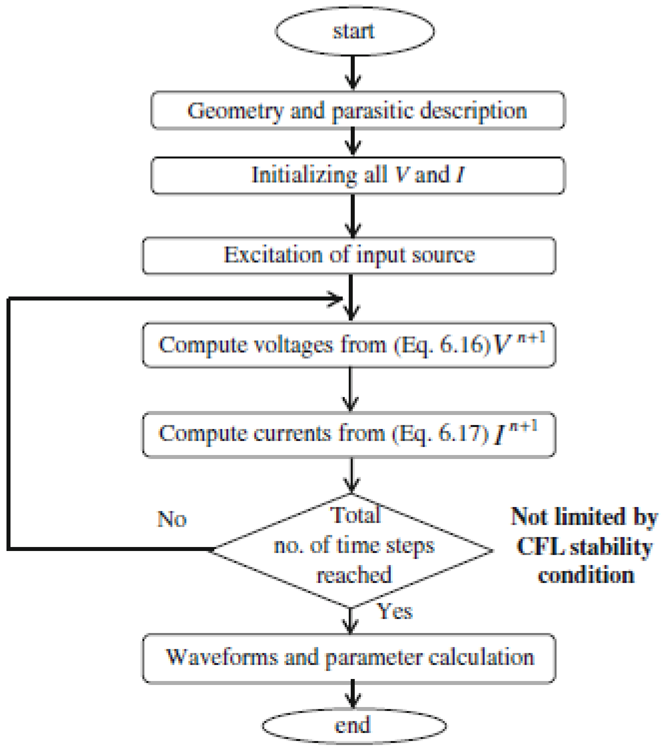

Figure 5.2: Flowchart of US-FDTD technique

The transient analysis has been performed using US-FDTD as shown in Fig.5.3. It is further compared with FDTD output and the HSPICE simulation. As it can be observed that the US-FDTD result lie close to simulation results with error less than 1 percent. Further the error percentage of US-FDTD is less than FDTD. The parasitics for copper have been taken from [32] [33]. The technology used for the analysis is 22nm. The aspect ratio considered for CMOS transistor is 2:1 and the capacitive load is taken as 2fF. The input given is a falling ramp signal from 0.9V to 0V.

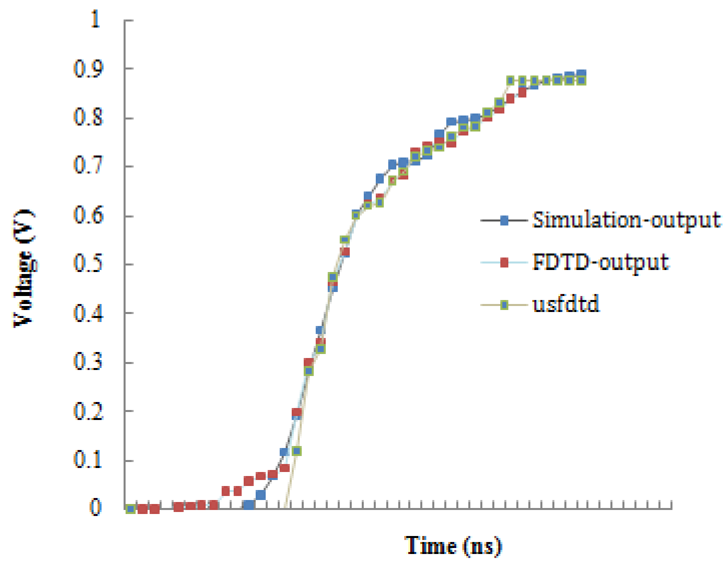

Figure 5.3: Transient analysis using US-FDTD technique

CHAPTER 6

Neural Network based Performance Evaluation of On-Chip Interconnect System

With different sizes of interconnects being employed for IC designs, it is necessary that in order to have a reliable performance one must be aware and conscious about increasing length on the output. Since, using the conventional methods of performance evaluation would result in time consuming process when employed on advanced technology, an alternative method is proposed namely NN. The developed method relies on dataset which determines the input and output parameters. Thus, NN lies in the category of supervised machine learning algorithm. The proposed method is developed using the following methodology as depicted in Fig. 6.1.

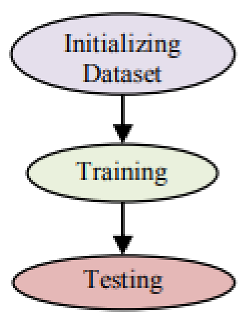

Figure 6.1: Flow chart representation of NN based model development

The detailed steps for NN based model for on-chip interconnect system are shown in Fig. 6.2. The first step involves dataset creation. In the current study, this is obtained using SPICE simulation that is implemented on driver interconnect model (DIL) model The DIL model is shown in Fig. 6.3. In this, the driver is a CMOS inverter and capacitor is taken as load. The next step consists of NN model creation. Thus, it is necessary to have an idea of its structure. The NN model consists of three layers namely input, hidden and output. Each of these layers contains nodes termed as neurons. These neurons are connected to each other with some strength known as weight. This is depicted in Fig.6.4. The inputs are given to the input layer of NN which are passed through the hidden layer and finally the result is obtained at the output layer. The hidden layer is responsible to convert the given data into mathematical form which the machine can comprehend and provide the required output from given input without any relation defined beforehand.

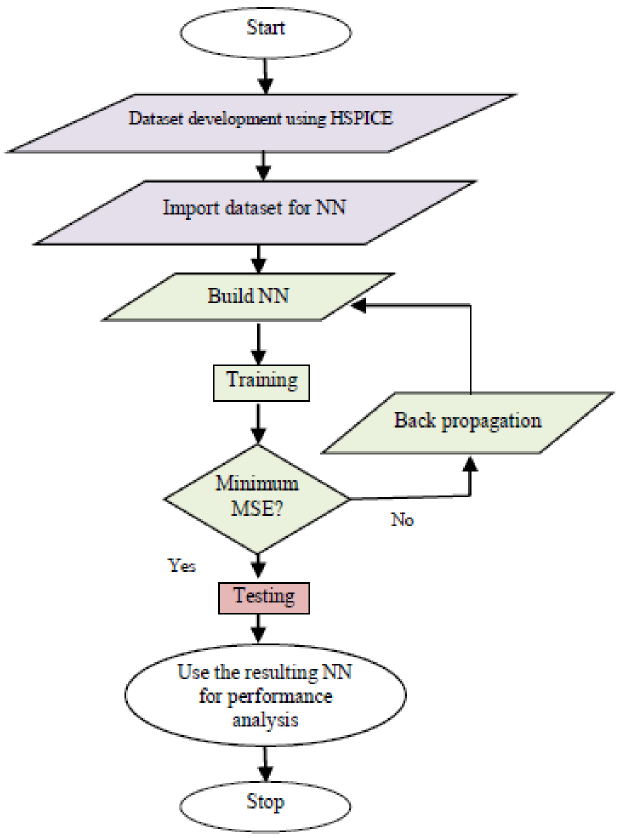

Figure 6.2: Procedural Steps of NN based model creation for performance evaluation for on-chip interconnect system.

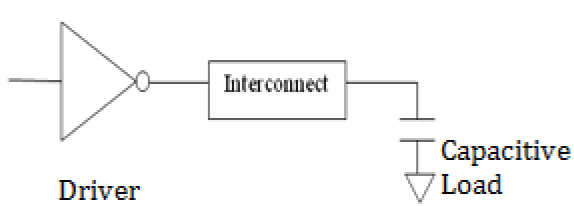

Figure 6.3: Driver-interconnect-load (DIL) model.

In Fig. 6.5., consider the output from the node of the hidden layer to be Z_i, the weights connecting to input layer as W_j, input node values as X_j and bias given as b, then Z can be expressed as:

$$Z_{ij} = \sum_{j=1}^{N} (W_j, X_j) + b \tag{6.1}$$

Here i and j are integer values representing the node number of hidden and input layers respectively

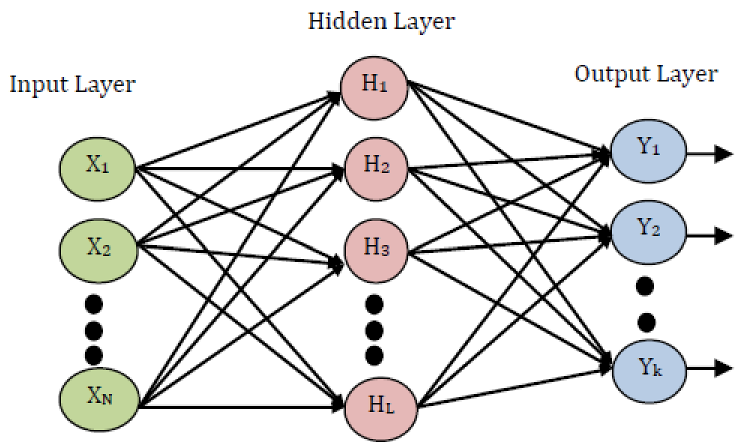

Figure 6.4: Neural network architecture

Bias is given so that output is not limited to origin and is flexible. After the output Z is obtained, it is passed through an activation function that incorporates appropriate non-linearity in order to improve its adjustability with any type of dataset.

The output 'Y' from output layer is obtained after 'Z' passes through the activation function. This can be denoted as:

$$Y_i = f(Z_i) \tag{6.2}$$

The activation function used for this study is sigmoid which is defined as [39]

$$f(Z_i) = \frac{1}{1 + e^{Z_j}} \tag{6.3}$$

In the training process, the normalized dataset is used to define a relationship between input and output variables. While creating the network, weights and biases are chosen at random. These weights are updated using back-propagation (BP) technique. In this technique, the predicted output is compared with the actual output in terms of performance parameter such as mean square error (MSE).

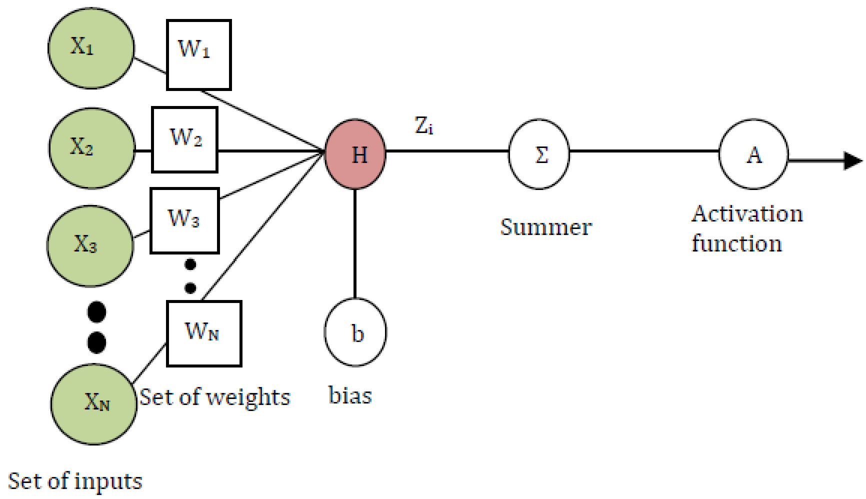

Figure 6.5: Detailed structure with respect to single neuron in hidden layer

Then the weights and biases are readjusted and compared again until minimum MSE is obtained. The readjustment is performed by employing algorithms such as gradient descent, Quasi Newton, Levenberg-Marquardt (LM) etc. This research work utilizes LM algorithm since it gives efficient trade-off between space and time complexity [43].Weight updation using LM algorithm is defined as:

$$W_{K+1} = W_k - (J_k^T.J_k + \mu I)^{-1} J_k.e_k \tag{6.4}$$

where J represents the Jacobian matrix, I is the identity matrix and e denotes the error matrix. k, T, μ refer to iteration index, transpose of a matrix and combinational coefficient respectively. The combinational coefficient is always positive. The LM algorithm is a derived using Gauss–Newton and steepest descent algorithms . If μ in equation (6.4) is very small or negligible, then equation (6.4) behaves like Gauss–Newton algorithm. On the other hand when is very large, equation (6.4) tends towards steepest descent algorithm. The complexity of LM algorithm depends on the Jacobian matrix and therefore the complexity of the proposed system depends on the number of input, hidden, output layers and on the number of neurons in the hidden layer. In training process, parameters and hyper-parameters are readjusted by employing the back-propagation algorithm. The parameters refer to weight and bias values which affect the accuracy of the NN network whereas the hyper-parameters include learning rate which affects the time taken to converge the model to a minimum error. Once the parameters and hyper-parameters are set and the network is validated, testing process occurs.

The next phase in training process is validation. It is during this phase that hyper parameters are updated. After training is the testing phase in which a different set of data is given to the network and mean square error is calculated in order to check the accuracy of the model.

6.1 Results and Discussion

The input parameters are electrical parasitics of interconnects namely resistance (r), inductance (l) and conductance (c) whereas the output parameters are delay and power dissipation. The r, l and c values are varied according to the length with minimum 500μm and maximum 3000μm. Number of samples taken are 2500 in which 70 percent is used as training samples, 15 percent as validation dataset and 15 percent as testing dataset. LM algorithm is used to update the weights in a continuous iterative process which occurs during backpropogation. The activation function employed is sigmoid

6.1.1 Validation of Developed NN Model

Regression curve reflects the closeness of the predicted and actual results. Regression coefficient (R) lies within the range of 0 to 1. The larger the R value, the greater is the accuracy. It can be observed from Fig. 6.6. that the developed model works considerably accurate in reference with actual results as the best fit line closely coincides with target and R is unity for each of the training, testing and entire datasets. Mean square error plot is shown in Fig. 6.7. It can be seen than after 35 iterations (epochs), mean square error is obtained which is negligible in value. Hence, system stabilizes and can be used with good accuracy after 35 iterations.

Further, error histogram in Fig. 6.8. depicts that the maximum dataset coincides with zero error line. The x axis shows the error whereas the y axis portrays the number of samples. Different colors are used to differentiate between training, validation and testing. These show that the developed NN based model possesses very less error and is highly accurate.

6.1.2 Performance Evaluation of On-chip Interconnect System using NN Model

After the NN network is validated and its structure is verified, performance analysis is implemented with varying interconnect lengths. The parameters considered

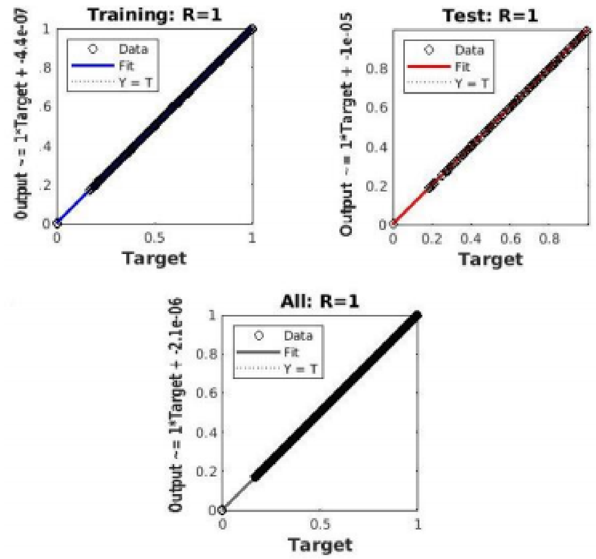

Figure 6.6: Regression curve for the considered model

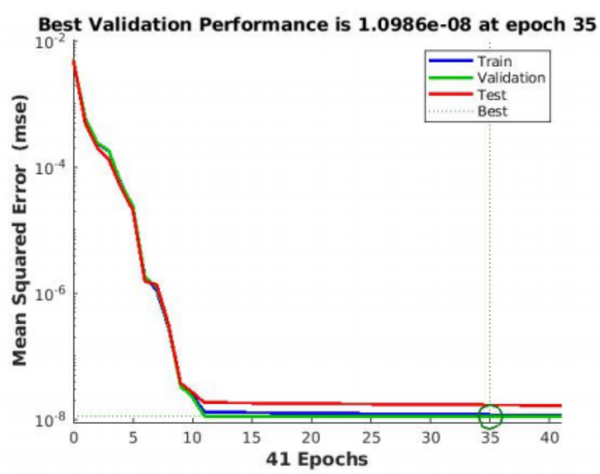

Figure 6.7: Mean square error plot

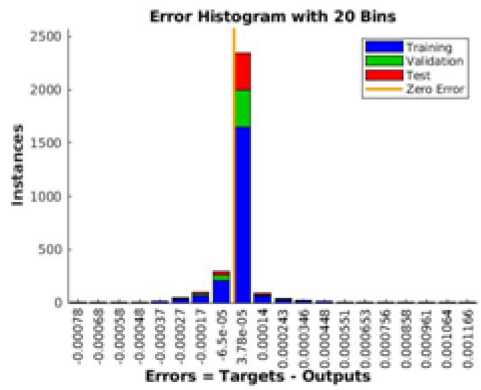

Figure 6.8: Error histogram

to evaluate the performance are delay and power dissipation. These are depicted in Figs. 6.9 and 6.10 respectively. Fig. 6.9 shows the delay plot with different interconnect lengths. It is seen that delay increases with interconnect length. This is because of the increasing parasitic values with the longer on-chip wire length. The results obtained from the proposed NN based model is compared with the SPICE simulation results. It is analyzed that the NN based model is highly accurate and has maximum error less than 5 percent. The power dissipation plot with interconnect length is shown in Fig. 6.10. It is seen that power dissipation also increases with interconnect length due to its increasing parasitics. Encouragingly, it is envisaged that the proposed NN based model is in good agreement with the SPICE results for all set of values.

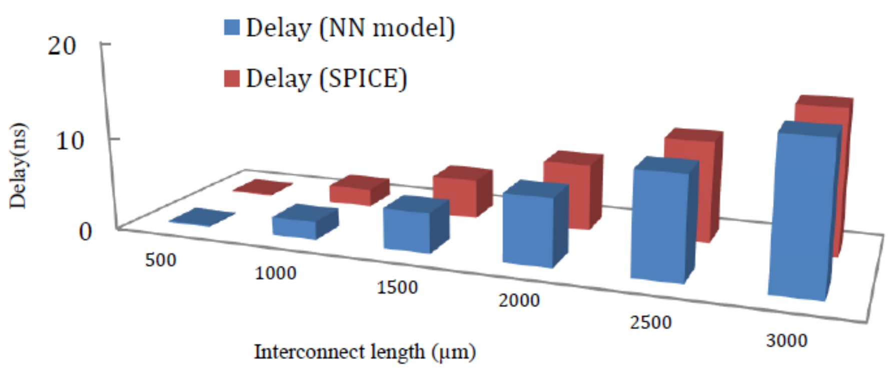

Figure 6.9: Delay comparison between simulation and proposed NN based model.

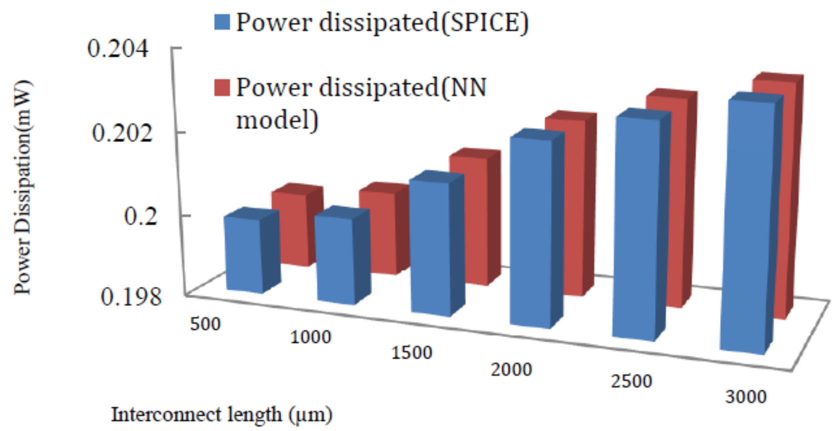

Figure 6.10: Power dissipation comparison between simulation and proposed NN based model.

6.1.3 Computation Time

In this section, time taken to predict performance using proposed NN based and conventional SPICE methods is analyzed. This is shown in Fig. 6.11. It is observed from the figure that time consumed for evaluating the required performance output results through the NN design is much lesser as compared to conventional SPICE method. It is investigated that the computation efficiency in terms of time requirement using the proposed NN based model is nearly five times greater than SPICE. Hence, NN based model can be convincely employed as a suitable method for performance evaluation of system with good overall performance efficiency.

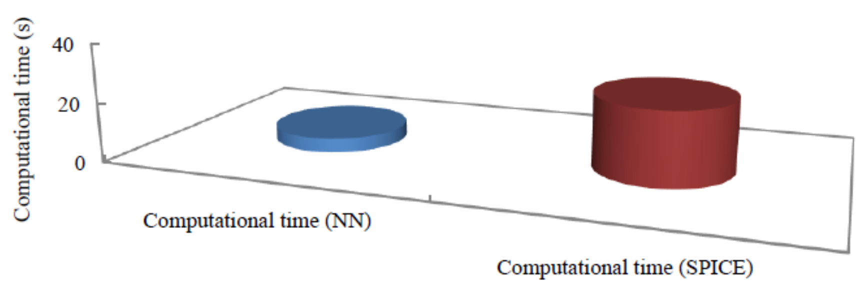

Figure 6.11: Comparison of computational time requirement for SPICE and NN based models

Chapter 7
Neural Network based Optimized Designing of On-Chip Interconnect System

This objective aims to create an automated design methodology in order to optimize the aspect ratio of the driver for the on-chip interconnect system. This automation is performed by employing ANN technique. The training and testing sets are created using HSPICE. After the validation of the network, the optimum aspect ratio is obtained by providing the desired performance attributes as input. NN based model is prominently able to design the system by determining optimum aspect ratio of drivers based on load and output performance requirements.

7.1 Model Formulation

7.2 Driver-interconnect-load (DIL) Model and Parasitic Extraction

For on-chip interconnects, driver that energizes interconnects and load that follows interconnects are important. Hence, the comprehensive model known as driver-interconnect-load (DIL) is usually considered for effective analysis and inference. This is shown in Fig. 7.1. In DIL system, both driver and load are often modeled as CMOS inverter. The CMOS inverter as load is electrically modeled as capacitive element. In CMOS driver, the physical dimensions of transistors i.e. width and length, or equivalently aspect ratio (width/length) are very significant parameters to define current over interconnect [44]. These essentially are also responsible for delineating delay and power dissipation in the system.

The interconnect material considered in the DIL model is copper. The copper interconnects can be electrically represented as transmission line model. It comprises of distributed structure of resistance (R), capacitance (C) and inductance

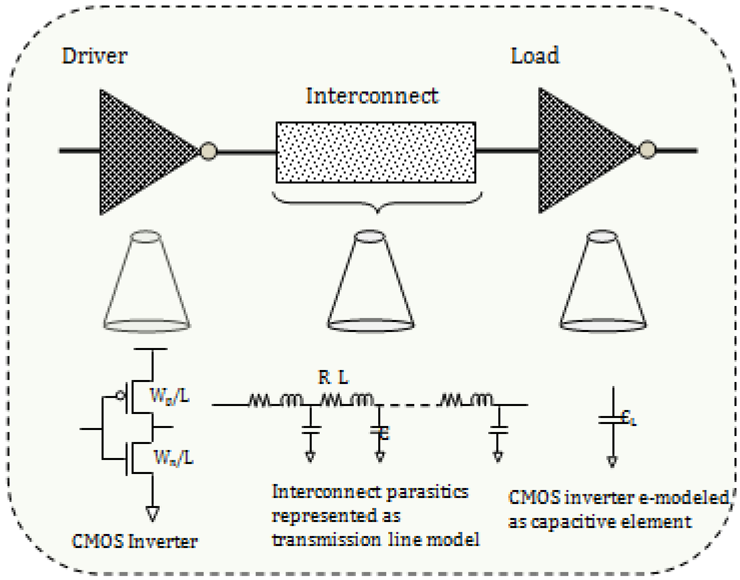

Figure 7.1: Driver-interconnect-load (DIL) model.

(L). These parasitics are determined as follows [32] [33]:

$$R = \frac{\rho l}{w.t} \tag{7.1}$$

Here ρ is the resistivity of the material. Its value is 2.2 $\mu\Omega$ -cm in case of copper [33]. Further, l, w and t refer to length, width and thickness respectively.

$$L = \frac{\mu_0.I}{2\pi}[ln(\frac{2l}{w+t}) + \frac{1}{2} + \frac{0.22(w+t)}{l}] \tag{7.2}$$

$$C_g = \epsilon[\frac{w}{h} + 2.22(\frac{s}{s+0.7h})^{3.19} + 1.17(\frac{s}{s+1.5h})^{0.76}.(\frac{t}{t+4.53h})^{0.12}] \tag{7.3}$$

$$C_c = \epsilon[1.14\frac{t}{s}(\frac{h}{h+2.06s})^{0.09} + 0.74(\frac{w}{w+1.59s})^{1.14} + 1.16(\frac{w}{w+1.87s})^{0.16}.(\frac{h}{h+0.98s})^{1.18}] \tag{7.4}$$

$$C_{total} = C_g + 2C_c \tag{7.5}$$

Here C_g is the area and fringe capacitance whereas the coupling capacitance is given by C_c. C_{total}refers to the total capacitance which is due the cumulative effect of C_g and C_c.

7.2.1 Development of Neural Network based Model

The process flow steps for the proposed model have been shown in Fig 7.2

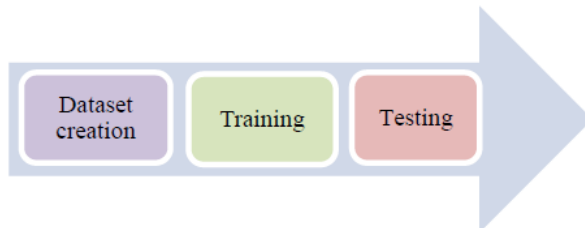

Figure 7.2: Process flow steps for NN based model development.

In this, the NN model that is created during training phase is used and no internal parameters are changed. A new dataset is considered to test the accuracy of the automated model. The results are compared with the actual dataset and the accuracy of the network is validated. Once the NN has been established and validated, it can be utilized for designing, optimization, and performance evaluation purposes. In the present study, the model that is employed for performance evaluation using constructed NN is depicted in Fig. 7.3. A different dataset with varying parameters is provided as input to the NN. In this case, the weights that are updated and obtained during the training phase is retained and not changed. At the termination-end of NN, desired output is obtained through which further system analysis can be performed.

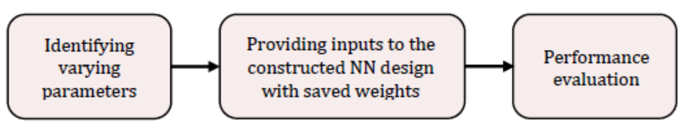

Figure 7.3: Model for performance evaluation of the system using NN design.

7.3 Results and Discussion

The dataset used in this research work is created using HSPICE and consists of delay, power dissipation and power-delay product corresponding to particular aspect ratio of the driving CMOS inverter. The width of the NMOS is varied from

22nm to 1μm and the length is kept constant. The aspect ratio between PMOS and NMOS transistors is taken as 2:1. Number of samples taken are 2000 which include 70 percent as training dataset, 15 percent as validation and the remaining 15 percent as testing samples. Back propagation is implemented for updating parameters using LM algorithm. Then Sigmoid is used as the activation function to maintain the non-linearity between output and input parameters. In the DIL model, CMOS inverter is considered as the driver. Copper is considered as on-chip interconnect material and characterized by transmission line model. The dimensions of interconnects are determined using ITRS [33]. The parasitics of copper interconnects are evaluated using PTM [32]. The value of resistance, capacitance and inductance are 151.5 kΩ/m, 15.114 pF/m and 1.654 μH/m respectively.

7.3.1 Assessing Accuracy of the Proposed NN based Model

Regression: The regression is the statistical process by which a relation is determined between output (dependent) and input (independent) parameters. The regression model is associated with the regression coefficient 'R' that determines the closeness between the output and input parameters. The value of R can vary from 0 to +1. Zero value of R indicates that there exists no linear relationship between the actual and predicted values whereas if R is 1 then, it reflects the high degree of correlation between actual and predicted values. In the present case, the regression model is used for the constructed NN based design to determine its accuracy. This is shown in Fig. 7.4. The output and input parameters considered are PMOS width and performance parameters respectively. In the figure, the regression curve is plotted for the entire dataset comprising of training, testing and validation phase. The normalized output dataset is plotted with respect to normalized target dataset. The Y axis denoted as output represents the predicted PMOS width obtained through the created neural network whereas the X axis denoted as target represents the actual PMOS width obtained through HSPICE dataset. The regression line shown in the figure gives a pictorial view of the closeness of the actual and predicted dataset. It is analyzed from the figure that the actual dataset is at 45 degree slope. This refers to the ideal condition where the output dataset is equal to the target dataset. Moreover, regression coefficient (R) has been determined for individually training, testing, validation and combinely overall phases. The values of 'R' for all these cases are 0.98139, 0.98766, 0.96298 and 0.9765 respectively. It is envisaged that for all the cases, 'R' is very close to unity. This shows the highly accurate and reliable characteristics of the proposed NN based model for the considered DIL system. It signifies that the NN based model is correctly trained and works accurately compared to the pre-existing methodology.

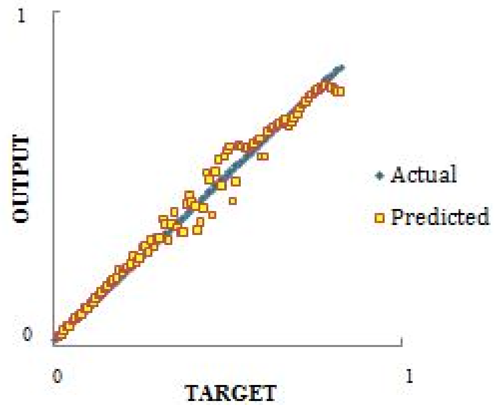

Figure 7.4: Regression curve for the considered DIL model.

Mean square error (MSE): MSE is used to measure the difference between the actual and predicted values. Analytically, MSE is determined by taking the average of the square of the errors and can be expressed as:

$$MSE = \frac{1}{n} \sum (Output_{actual} - Output_{predicted})^2 \tag{7.6}$$

The MSE value should be towards lower end for accurate systems. The MSE is evaluated for different phases namely train, test and validation. The MSE is iteratively evaluated and based on these values, weights of the NN are updated in each cycle using LM back-propagation algorithm. The back-propagation implementation is made stopped once MSE reaches to lowest value and remains constant for all the phases. For the present case, MSE is plotted and shown in Fig. 8. From the figure, it is seen that MSE becomes constant at around 2.1695 * 10^{-18}. This MSE value is obtained after 588 iterations and correspondingly 8 seconds. This signifies that the developed NN based model stabilizes and becomes considerable in 8seconds.

Error histogram: This defines the frequency of occurrence of different values of errors. This is another effective measure for evaluating accuracy of the system. The error histogram for the present case is shown in Fig. 9. In the present case, total data inputs considered are 2000. For all this set of data, it is investigated that error varied from -5.2 * 10^{-9} to +3.64 *10^{-9}. This is represented on x-axis of Fig. 7.6. Thereafter, the occurrence of each error value is plotted. The error is

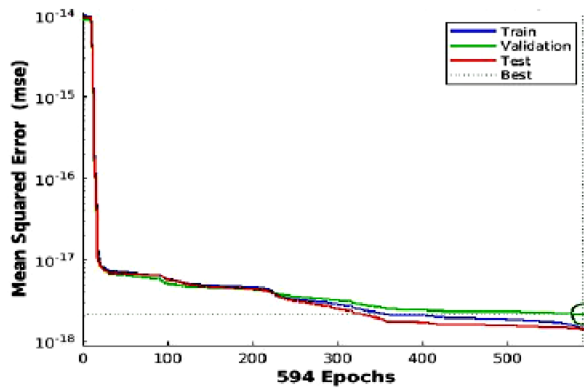

Figure 7.5: Mean Square error plot for the considered DIL model.

calculated as:

$$error = target - output \tag{7.7}$$

From the figure, it is observed that the error histogram follows the Gaussian curve. It is inferred from the figure that for most of the input values, error is negligible. This is evident from Fig. 7.6 where maximum occurrence of error lies near the zero error line. It is investigated that the maximum occurrence of error is at -2.81 $*10^{-10}$. This low value of maximum error signifies the correctness of the developed NN based model.

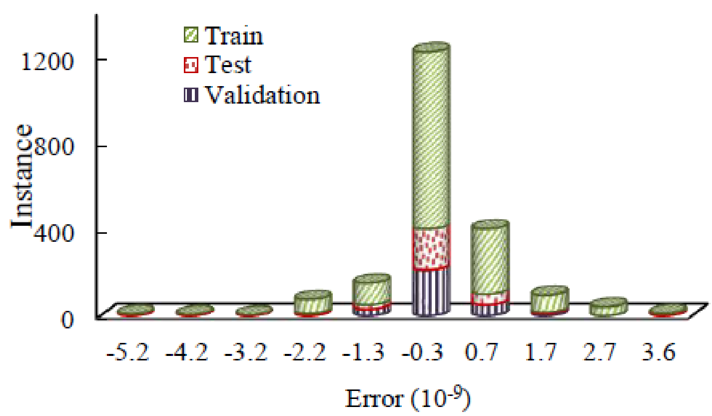

Figure 7.6: Error histogram plot for the considered DIL model

7.3.2 Varying delay and power requirements

In this case, the system is designed for varying delay and power requirements. This analysis is beneficial for essential applications that require particularly either low delay, low power dissipation or some trade-off between the two. Using this analysis, optimum designing of the circuits can be efficiently determined using the proposed NN based model. In the present DIL model, the design parameter is aspect ratio i.e. 'Width/Length' of PMOS and NMOS transistors in the CMOS inverter driver. The range of the delay constraint is kept as from 0.1 ns to 5 ns while the range for power dissipation variation is made from 0.1 μ W to 2 μW. This wide range is chosen keeping in view the different possible desired requirements of output performance parameters. Fig.7.7. depicts the actual and predicted width of the NMOS transistor of inverter in DIL model corresponding to the different output performance parameters which are selected at random from the dataset. The channel length of the transistor is fixed as 22nm and the ratio between PMOS and NMOS is considered as 2:1. Thus, the predicted PMOS width will be twice the predicted NMOS width. Further fig.7.8. represents the percentage error between the actual and predicted values of NMOS width. It is analyzed that the average percentage error for all the considered cases is 1.67 percent. The low value of percentage error reflects the high accuracy of the proposed NN based model.

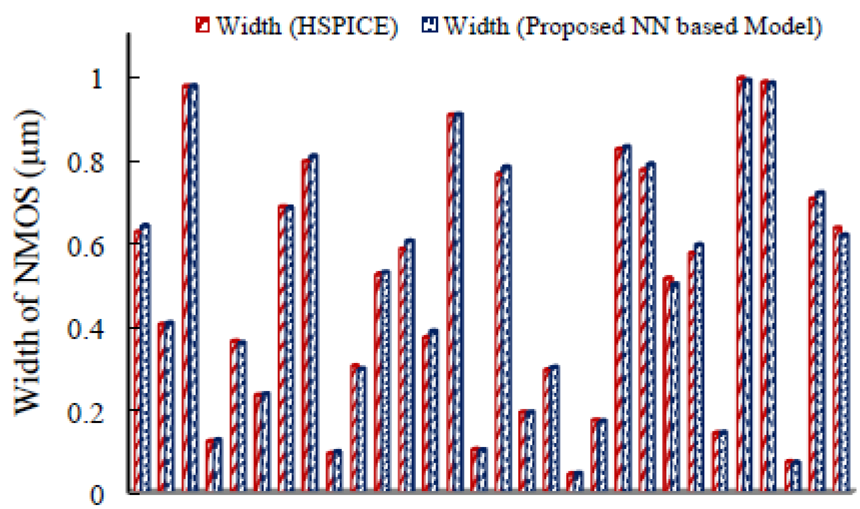

Figure 7.7: Comparision between actual and predicted optimized NMOS width

7.3.3 Varying loading requirements

The considered DIL model comprises of capacitive load that is electrically model representation of CMOS inverter. In practice, the number of gates driven by on-chip interconnects may vary. Depending on the gates driven by interconnects at output, the value of equivalent loading capacitance and output current varies. This also affects the output performance such as delay and power-dissipation. Fig.

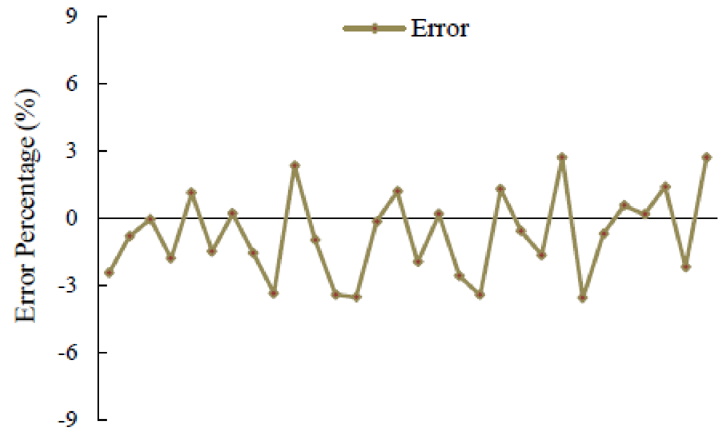

Figure 7.8: Percentage error between predicted and actual NMOS width

7.9. shows the effect of varying capacitive load on output performance parameters. The loading capacitance is varied from 2 fF to 10 fF. It is analyzed that both delay and power-dissipation increases with increase in the loading capacitance.

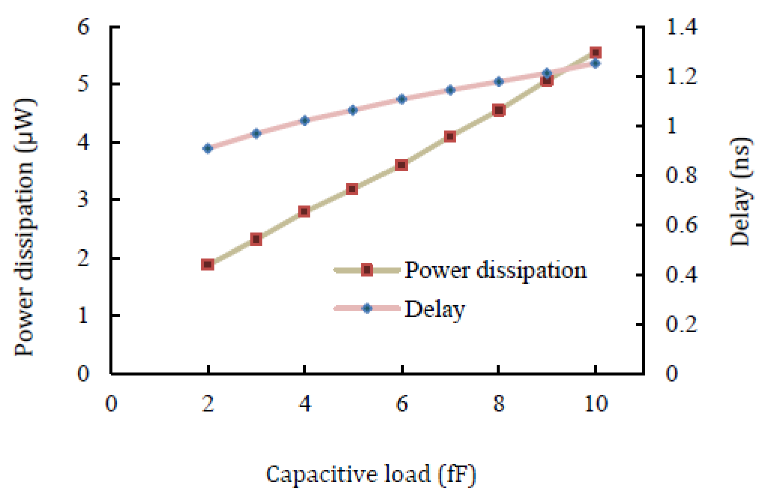

Figure 7.9: Effect of variation of capacitive load on delay and power-dissipation

In order to efficiently drive the particular load and deliver sinking output current, the driver of the DIL system need to be designed optimally. This can be suitably designed using proposed NN based model. For the present discussed case, the capacitive load value in the DIL model (Fig. 7.1) changes from 2fF to 10fF. The delay and power dissipation is kept constant at 1.77ns and 1.01W. The parameters are adjusted after 146 iterations to give the best performance. The R value for training, testing, validation and overall period is determined as 0.99997, 0.99992, 0.99992 and 0.99996 respectively. The NMOS width of transistors of CMOS driver inverter is determined using developed NN. Fig. 7.10 shows the obtained NMOS width for different loading values. From the figure it is seen that with increase in loading, the NMOS width tends to increase and then decrease such that the defined performance in terms of delay and power dissipation is maintained.

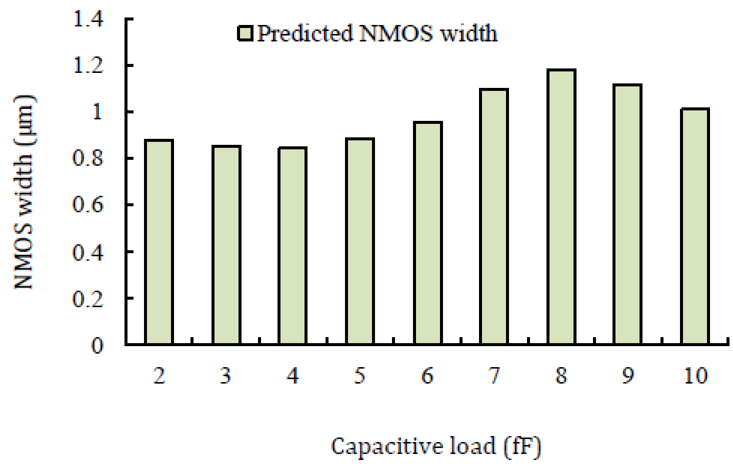

Figure 7.10: NMOS width prediction of driver in DIL model using proposed NN based model for defined performance parameters.

7.3.4 Effect of varying aspect ratio of driving transistors

The performance parameters namely delay and power dissipation for varying aspect ratio of driving transistors are predicted using NN based model and compared with the actual dataset. This has been shown in Fig. 7.11. The interconnect length is kept constant as 1mm. It can be observed from figure that on increasing the width of NMOS the delay reduces whereas the power dissipation increases. This is because as width of transistor increases, correspondingly the driving current increases. Higher current leads to faster switching of circuit resulting is smaller delay. On the other hand, higher current leads to more I2R losses that causes higher power-dissipation in the circuit. Also the obtained results from proposed NN based model is validated using actual HPSICE data. It is analyzed that the maximum percentage error between the two is less than 1.6 percent . The low value of the percentage error shows the accuracy and efficacy of the proposed NN based model in determining the output performance of the considered DIL system.

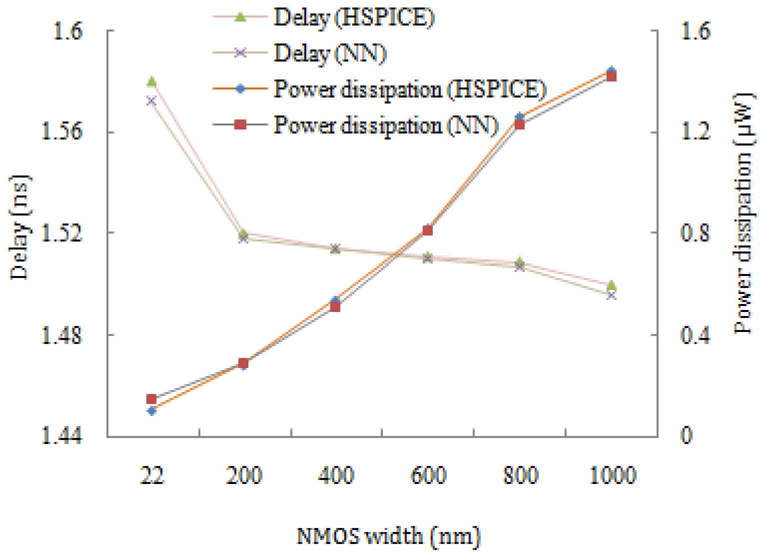

Figure 7.11: Delay and power dissipation assessment with variation in channel width of driver transistor in DIL model.

CHAPTER 8

Variability Analysis using Neural Network Technique

At scaled technology nodes, interconnects are the major governing parameter in determining the efficiency of electronic devices. At lower technology nodes, the non ideal effect such as variability also aggravates substantially. The term variability refers to fluctuations in parameters due to variations in process, voltage, temperature etc. which results fluctuations in output system performance. Variability analysis can be accomplished using several statistical mathematical techniques such as Monte Carlo, parametric analysis, process corner, ANOVA and rank table analyses. However, these conventional techniques are becoming obsolete and deficient in determining the severe variability effects of the sophisticated, densely-packed and enormously large on-chip interconnects. Moreover traditional techniques are tremendously computational expensive. Henceforth in the present work, the prospective neural network based on back propagation captures the effect of highly variable parameters that are existing in on-chip interconnects. Back propagation neural network (BPNN) is used with Levenberg–Marquardt (LM) algorithm to adjust weights of hidden layer in order to minimize error. The proposed model is efficient and versatile such that it predicts the reliability of the circuit performance based on circuit parameters such as resistance, inductance and capacitance values in much lesser time. The performance parameter considered for the developed model is mean square error. This section presents the results that are obtained using the developed model that is based on NN approach. The precision of the developed model is also compared with the traditional analytical model. The ANN based model is developed for 32nm technology using. The on-chip interconnect dimensions are defined in the Table 1 [9] [10].

The neural network is trained using dataset that is generated from Monte Carlo simulations. These have been performed using HSPICE. Interconnect parasitics namely resistance, inductance and capacitance are varied. The output per-

Interconnect Dimension	Value
Width(w)	48nm
Space(s)	48nm
Thickness(t)	144nm
Height(h)	110.4nm
Aspect Ratio	3
Vdd	0.9V
Length	0.5mm
Dielectric Constant(ϵ)	2.25

Table 8.1: Interconnect dimensions for 32nm technology

formance parameters are delay and power dissipated. The interconnect length considered is 0.5mm. The Monte Carlo simulations have been performed for 1000 iterations. The process parameters are varied with a deviation of $\pm$ 10 percent simultaneously. Further training, testing and creation of neural network structure have been implemented in MATLAB with the help of nntraintool. Training dataset consists of 70 percent of the total dataset. Further the remaining dataset is divided into validation set and testing dataset each with 15 percent of the total dataset. Input layer is connected to hidden layer. Number of hidden layers and neurons in it depend on the complexity of the problem. Since Feed forward neural network does not have any prior knowledge regarding the weights or hidden layers, henceforth back propagation algorithm is used to compute weights. These weights are iteratively updated in order to fit with respect to the performance parameter. For this problem, two hidden layers have been employed with count of neuron number as 10 and 8 respectively. The training algorithm used in LM algorithm with 1000 epochs (iterations) and mean square error as a performance parameter. The activation function used is sigmoid in order to introduce non-linearity to the hidden layer.

8.1 Validation and accuracy assessment of the developed NN based model

The regression plots are shown in Figures 8.1,8.2 and 8.3.

Further mean square error and error histogram have been plotted in Figure 8.4 and Figure 8.5 in which it can been seen that after 32 epochs or iterations best performance of neural network is obtained. Also maximum numbers of samples have nearly zero error.

After the created NN functionality is validated , variability analysis is done

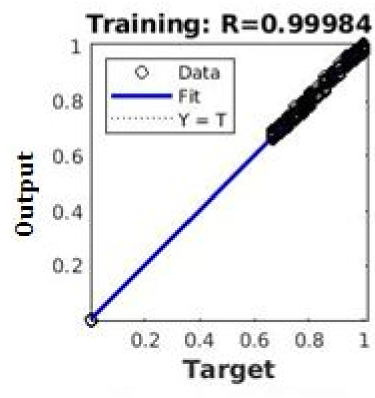

Figure 8.1: Training regression plot

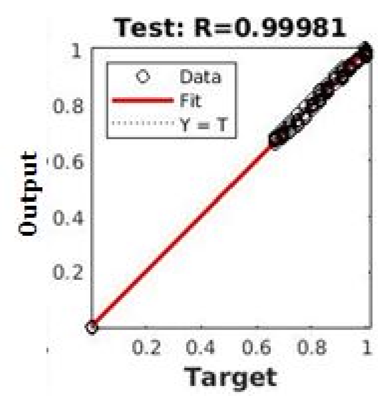

Figure 8.2: Testing regression plot

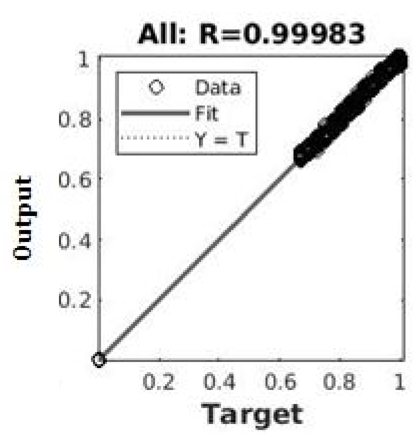

Figure 8.3: Regression plot for entire data.

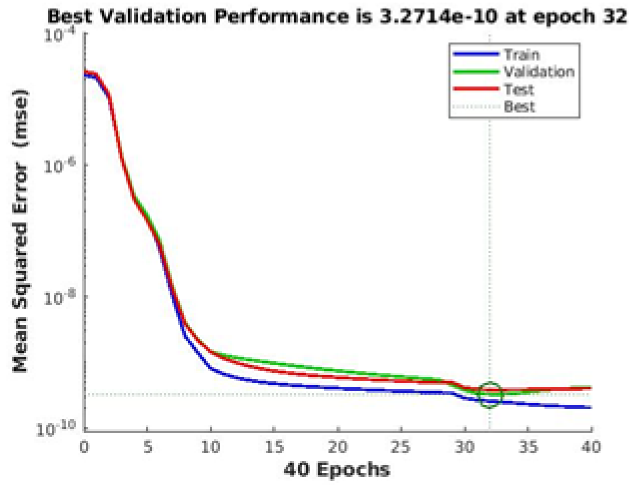

Figure 8.4: Mean square error plot.

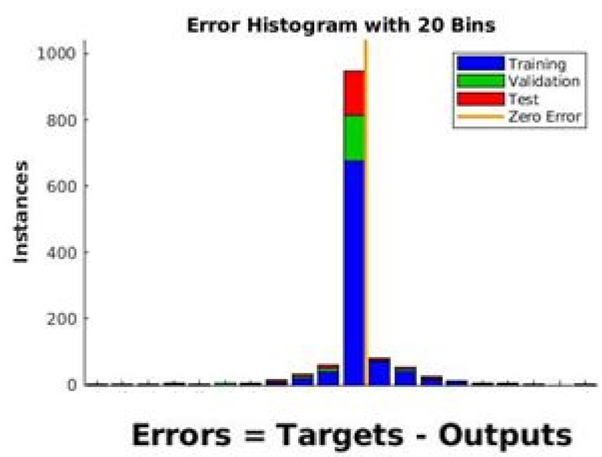

Figure 8.5: Error Histogram plot

with ± 10 percent variation in input parasitics to create testing dataset. This process is done for different interconnect lengths and compared with the traditional Monte Carlo method in terms of mean power dissipation and delay. This is depicted in Figure 8.6.and Figure 8.7.

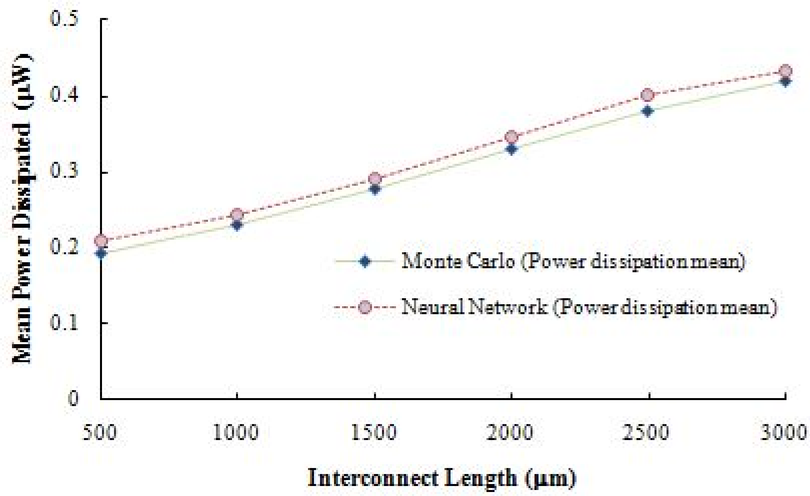

Figure 8.6: Monte Carlo and NN comparison plot based on power dissipation

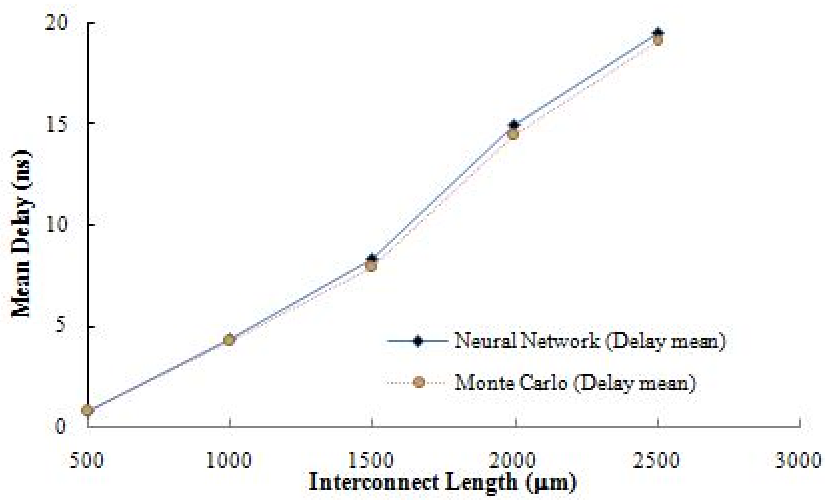

Figure 8.7: Monte Carlo and NN comparison plot based on delay

Further the computational time is compared between the proposed and the conventional method as shown in Figure 8.8. As it can be observed the computational time is much less for Neural network

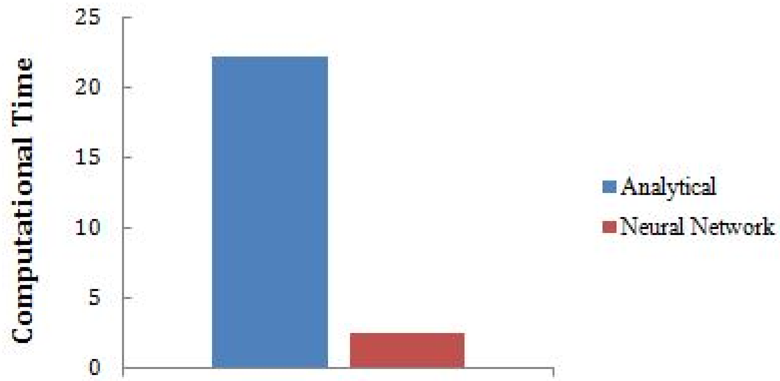

Figure 8.8: Monte Carlo and NN total time elapsed plot

CHAPTER 9

Performance Analysis of Graphene Interconnects with Graphene MOSFET

Graphene is one of the allotropes of carbon which is being explored as an alternative to the existing copper interconnect. Graphene can form of graphene nanoribbon (GNR) when its width is lesser than 50nm. They possesses improved electrical and mechanical properties when compared to the present interconnect materials. GNR can be classified on the basis of their orientation as armchair (ac-GNR) or zigzag GNR (zz-GNR). [45] Zz-GNR are always metallic in nature whereas ac-GNR can be metallic or semi-conducting in nature. Ac-GNR can be termed as metallic in nature if number of carbon atom N along its width are N = 3p-1 or N = 3p+2 where p can be any integer (p=1,2,...). Further ac-GNR is semi-conducting when N = 3p or N = 3p+1.

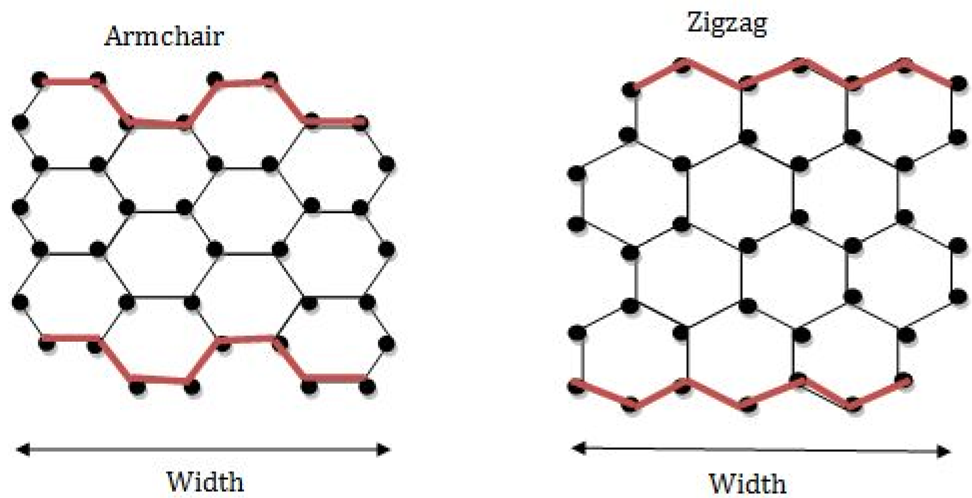

Figure 9.1: Armchair and zigzag structures of MLGNR

GNR is classified as multilayer GNR (MLGNR) and single layer GNR (SLGNR) depending on the number of graphene sheets used. MLGNR is preferred usually since it provides better conductance and easier fabrication. MLGNR can be further classified as top contact MLGNR (TC-MLGNR) and side contact MLGNR (SC-MLGNR). Since contact resistance is lower in SC-MLGNR, it is preferred over TC-MLGNR [46]. The structure for SC-MLGNR has been depicted in Fig. 9.1.

9.1 MLGNR Interconnect

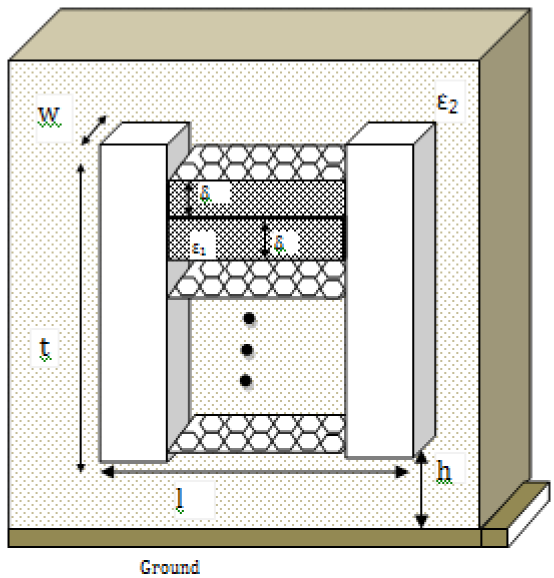

Figure 9.2: Schematic representation of MLGNR interconnect over ground plane.

SC-MLGNR consists of multiple GNR layers stacked on top of each other with a dielectric medium such as HfO_2, Al_2O_3 etc (represented as ϵ_1) between them [47], [48]. This prevents interlayer electron hopping thereby decreasing impedence and increasing electron hopping. The thickness between the nanoribbons is kept equal to Vander-waal's gap (δ = 0.34nm) [49], [50]. This structure is enclosed in a dielectric medium, ϵ_2 such as SiO_2 dimensions w, t, l, h in Fig. 1 refer to width, thickness, length and height from the ground plane. The MLGNR interconnect can be represented by electrically equivalent single conductor (ESC) model. This is shown in Fig. 9.2. This comprises of various resistive, capacitive and inductive parasitics. The quantum resistance is the resistance of ideal quantum wire which considers zero scatering. It is denoted as

$$R_q = \frac{\hbar/2e^2}{N_{ch}} \tag{9.1}$$

Where $\hbar$ is the planck's constant, e is the electron charge and N_ch is the number of conducting channels present in a single layer. In real time scenario the scaterring, defects and rough edges exist. Also the mean free path is finite. In the figure, Rc_1 and Rc_2 represents the contact resistance and Rs is the scattering resistance which is represented as:

$$R_s = \frac{R_q}{l_{MFP}} \tag{9.2}$$

Where $l_M FP$ represents mean free path of an electron. The contact resistance exists due to imperfect contact between the metal and GNR layers and it is negligible. The equivalent resistance per unit length (R_N) for N-layer SC-MLGNR is given as:

$$R_N = \frac{R_s}{N} \tag{9.3}$$

Where N is the total number of layers in the MLGNR structure. It is defined as:

$$N = 1 + int\frac{t}{\delta} \tag{9.4}$$

Where t is the height of the interconnect and δ is the vander-wall's gap The total resistance R_S is given as

$$R_s = R_N + \frac{R_s + R_{C1} + R_{C2}}{N_{ch} * N} \tag{9.5}$$

Where RC_1, RC_2 are the side contact resistance of SC-MLGNR. , $N_c h$ refers to the total number of conducting channels present in a single layer. $N_c h$ is formed due to both conducting and valence conducting bands. It can be defined using Femi-Dirac function which can be defined as:

$$N_{ch} = \sum_{1}^{n_c}(1 + e^{\frac{(E_{in}-E_f)}{kT}})^{-1} + \sum_{1}^{n_v}(1 + e^{\frac{(E_{ih}-E_f)}{kT}})^{-1} \tag{9.6}$$

Where T is the temperature, k is the Boltzmann's constant, E_f represents the Fermi energy and E_{in} and E_{ih} n be defined as minimum energy in the i^{th} sub-band. This can be derived as shown in [46] The total inductance of the MLGNR interconnect is equivalent of kinetic inductance (L_k) and magnetic inductance (L_M). L_k and L_M can be calculated as follows [51]:

$$L_k = \frac{(\hbar/4e^2).v_f}{N.N_{ch}} \tag{9.7}$$

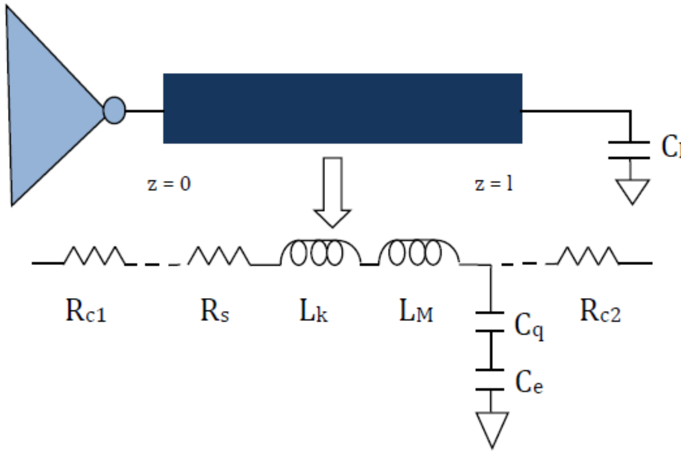

Figure 9.3: Electrical equivalent single conductor model of MLGNR interconnect

$$L_M = \frac{\mu d}{m} \tag{9.8}$$

$$L = L_M + L_K \tag{9.9}$$

where μ is the permeability of graphene Also the total capacitance in MLGNR is due to quantum capacitance (C_q) and electrostatic capacitance (C_e). This can be expressed as follows [49] [50]:

$$C_q = N.N_{ch}\frac{4.e^2}{\hbar.v_f} \tag{9.10}$$

$$C_e = \frac{w}{d} \tag{9.11}$$

$$C = \frac{C_q.C_e}{C_q + C_e} \tag{9.12}$$

where N_ch refers to the total number of conducting channels present in a single layer, ϵ refers to dielectric permittivity of graphene . As it can be seen that the electrostatic capacitance and magnetic inductance are dependent the interconnect geometry and surrounding dielectric material whereas the quantum capacitance and kinetic inductance are dependent on number of layers and number of channels in a layer of GNR interconnect. The kinetic inductance is dependent on inertia and mobile charge carriers. Since multiple interconnect structures are coupled with each other they have mutual inductance and capacitance which can be calculated by [49] [52].

9.2 GNR – Field Effect Transistor

On the basis of device structure GNRFETs are classified into two types known as SB-type and MOS-type GNRFETs. SB-type GNRFETs are fabricated using metal as contacts and graphene as channel. On the other hand, GNRFETs formed with reservoirs doped with n-type impurities (N-type GNRFET) and p-type impurities (P-type GNRFET) referred to MOS GNRFET. MOS-GNRFETs are favoured over SB type GNRFET due to high ratio of on and off current. To get the desired performance in a device amount of output current is need to be controlled and this current is controlled by the threshold voltage. Hence, it can be stated that control over threshold voltage is extremely important to achieve high performance. Due to fixed bandgap in conventional Si-MOSFET, the threshold voltage can only be controlled by different process parameters such as material of gate electrode, dielectric constant, thickness of oxide and substrate doping, whereas in GNR-FET bandgap engineering of GNR makes it to function at scaled technology. Symmetrical net effective mass of electrons and holes in GNRFET results exact equal and opposite response, hence design procedure of GNR-FET is much simpler than that of Si-FET circuits. Width of GNR is known as width of channel depends entirely on number of ribbons. Mathematically it can be expressed as

$$W_{ch} = (N+1) * 1.732 * (0.144/2) \tag{9.13}$$

9.3 Analysis of ON and OFF current in GNR-FET

Limitations of Si MOSFETs at lower technology node energized exploration of emerging devices that can not only maintain consistency with Moore's law but also reduce the leakage currents and henceforth OFF state current. Graphene nano-ribbon (GNR) FET is one such device that has been investigated as one of the most promising device. Owing to extremely high carrier mobility, excellent thermal strength, low parasitic capacitance and effective mass, GNRFET excellently performs at nano miniaturized technology nodes. Due to higher carrier mobility exhibit much more rapid response than that of conventional silicon based MOSFETs. The OFF state current in GNRFETs reduces as thickness of dielectric is reduced. Consequently, scaling of oxide thickness does not impact the overall performance of GNR FET as had been the case with Si FET. An MOS type GNR-FET with armchair chirality is considered in the present work. To improve the driving strength of GNRFET ribbons with armchair chirality are connected in parallel. As mentioned earlier MOSGNRFET are formed by doping of n-type and p-type impurities, the doped part is known as reservoirs whereas channel is formed by the intrinsic part. Similar to Si-FET phenomenon of turning on and off of device is controlled by gate terminal. Equivalent model of single GNR in SPICE is shown in Fig.9.4. Modelling of GNRFET circuit involves determination of channel capacitance, channel potential, intrinsic capacitance and also complicated approximation.

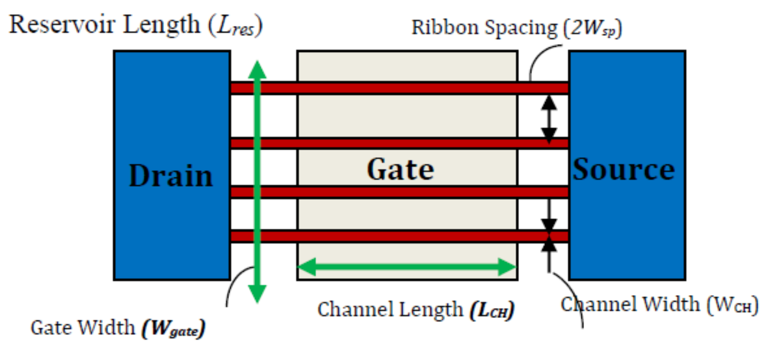

Figure 9.4: GNR FET Model

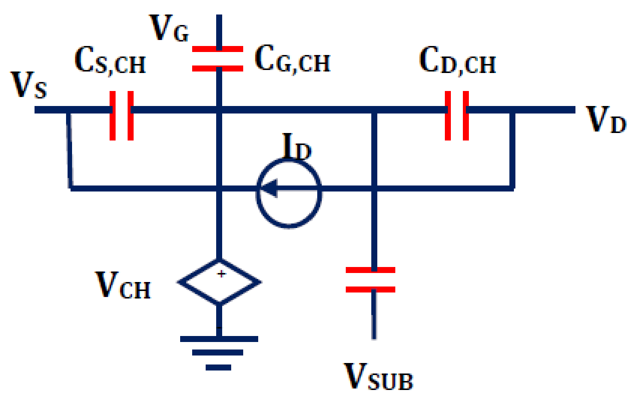

Figure 9.5: Detailed Structure of GNR with N=1

Entire calculation of different parameters as well as current is presented in [51]. Drain current in MOSGNRFET can be expressed as

$$I_e = \frac{2qkT}{h} \sum_{\alpha} [ln(1 + e^{\frac{(q(\psi_{ch}-V_S)-\epsilon_\alpha)}{kT}}) - ln(1 + e^{\frac{(q(\psi_{ch}-V_D)-\epsilon_\alpha)}{kT}})] \tag{9.14}$$

Where ψ_{CH} is channel potential, ϵ_α is sub band index, V_D is the drain potential, V_S is source potential, k is boltzman constant and T is room temperature. From

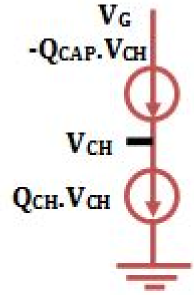

Figure 9.6: Circuit Set up to solve CH

the equation of current it can be stated that on current increasing the channel potential improves the magnitude. To find out the impact of thickness of dielectric and dielectric constant on ratio of on and off current SPICE set up for calculation of channel potential is taken under consideration [Fig.9.6]. Calculation of channel potential involves determination of physical capacitance (Q_{CAP}) and channel capacitance (Q_{CH}) as shown in Fig.9.6. Out of these value of physical capacitance depends on different capacitors such as capacitance between gate and channel as well as channel and substrate. During on state of device the equivalent capacitance due to gate terminal is gate and channel whereas in off state coupling occurs between gate and substrate. In both cases the oxide layer will act as dielectric layer, henceforth gate capacitance rely upon the thickness of oxide layer and its dielectric constant value. Mathematically Q_{CAP} can be expressed in terms of physical and channel capacitance as follows.

$$Q_{CAP} = C_{G,CH}(V_G - V_{FB} - \psi_{CH}) + C_{SUB,CH}(V_{SUB} - V_{FB} - \psi_{CH}) \tag{9.15}$$

Where C_G,C_H is gate to channel capacitance and C_{SUB},C_H is channel to substrate capacitance V_{FB} is flat band voltage, V_{SUB} is sub band voltage and V_G and V_S are gate and substrate voltage respectively. Gate to channel capacitance is defined as

$$C_{G(SUB),CH} = \frac{5.5 * 10^{-11}.\epsilon_r.L_{CH}}{(1+\frac{1.5t_{ox}}{W_G}).ln(\frac{5.98W_{CH}}{0.8t_{ox}})} \tag{9.16}$$

In which ϵ_r is dielectric constant, t_{ox} is thickness of oxide and W_{CH} and W_G are channel and gate width respectively. Therefore, from the above mentioned equations it is derived that as we increase the thickness of oxide, gate capacitance gets decreases which makes decrement of Q_{cap}. As stated earlier on current is directly proportional to channel capacitance and physical capacitance, it is inferred that on current reduces as we increase thickness of oxide. Henceforth we can say that scaling of thickness of oxide layer boost up the magnitude of on current. Now, following the effect of oxide thickness, influence of dielectric constant can be observed in same way. In the case of dielectric constant from equation 9.16 it is seen that gate capacitance increases as we raise the value of dielectric constant. This results in increment of value of Q_{CAP} and henceforth channel potential and on current. Thus, it is concluded that raising up the value of dielectric constant hikes the magnitude of on current. Off current of device is determined by substituting the value of gate voltage to zero as in this condition the device remain at cut off condition. Substituting the value of gate voltage to zero in equation results

$$Q_{CAP} = C_{SUB,CH}(V_{SUB} - V_{FB} - \psi_{CH}) + C_{G,SUB}(V_{SUB} + V_{FB}) \tag{9.17}$$

Now considering the equation 9.14 for off current analysis, it is observed that value of physical capacitance will decrease due to increment in gate to substrate capacitance. Henceforth off current will be at minima when the oxide thickness will be minimum.

9.4 Circuit Designing with GNR-FET and GNR interconnect

At lower technology node interconnects effects the performance of device and correspondingly frequency of device. Henceforth, it is necessary to analyse the impact of interconnects along with device in order to determine the signal degradation and performance. Delay and power of GNR-FET and Si-FET with copper and GNR interconnects is determined for Driver Interconnect Load Model (DIL) for all the combinations at 22nm technology node and it is concluded that GNR-FET with GNR interconnect results least delay and power dissipation. Length of interconnect is taken as 1um in the considered design and correspondingly value of resistance, capacitance and inductance is determined [53]. A mono ribbon GNR having values of R, L and C as 0.9k, 0.16nH and 0.00578fF are taken in the present design respectively. Table shows the delay and power of four different combination of DIL model that is Si-FET with copper interconnect, Si-FET with GNR interconnect, GNR-FET with copper interconnect and GNR-FET with GNR interconnect. The high mobility of carriers in GNR-FET than Si-FET and lower value of interconnect parameters of GNR than that of Copper results lesser interconnects delay results minimum delay. As proved in earlier section that leakage power in GNR-FET is significantly lower than that of Si-FET at lower technology node, henceforth GNR-FET with GNR interconnect model results least power dissipation also out of all combinations.

Device	Delay	Power Dissipation
Si-FET and Cu interconnect	7.890 x 10^{-9}	9.453 x 10^{-5}
Si-FET with GNR interconnect	7.69 x10^{-9}	8.649 x10^{-5}
GNR-FET with Cu interconnect	6.436 x10^{-9}	2.133 x10^{-5}
GNR-FET with GNR interconnect	2.975 x10^{-9}	1.344 x10^{-5}

Table 9.1: Delay and Power dissipation of DIL models

9.4.1 Design of Ring Oscillator with GNR-FET and GNR interconnect

Ring oscillator is a device which consists of odd number of stages of inverter connected in series and the output of last inverter is fed back to the input of first inverter. Ring oscillators are utilized in numerous applications such as in voltage control oscillators of Phase Locked Loop (PLL), random number generation, to find out the impact of voltage as well as temperature on chip etc. The output of ring oscillator oscillates between 0 and 1 and the frequency depends on the delay of each stage and no of stage. The frequency of ring oscillator can be determined analytically as

$$F = 1/2nT_d \tag{9.18}$$

Where T_d is defined as delay of single inverter in ring oscillator and n as no of inverters connecting together. A high frequency ring oscillator is desired in every application as higher frequency leads to generation of more data in a time period. A 3 stage ring oscillator is designed with Si-FET and GNR-FET and GNR as interconnect. Specifications of process parameters taken in the design mentioned in the table 9.2 [54] [55]

From the simulation results of DIL model and also a ring oscillator with specifications given above it is concluded that GNR-FET with GNR interconnect systems provides least delay and power as well as high frequency. Henceforth, therefore due to excellent performance and less power dissipation this configuration of

Parameters	GNR-FET	Si-FET
Gate Length (L_g)	22nm	22nm
Width of PMOS (W_p)	W_p = 2.123nm	W_p = 80nm
Width of NMOS (W_n)	W_n=2.123nm	W_n= 50nm
Dielectric Constant (K)	3.9 (SiO_2)	3.9 (SiO_2)
Thickness of Dielectric (T_{ox})	1nm	1nm
Supply Voltage (V_{dd})	1 volt	1 volt

Table 9.2: Process Parameters for GNR and Si FET

ring oscillator could be taken in voltage controlled oscillators.

Device	Frequency of Oscillation
Si-FET	9MHz
GNR-FET	10MHz

Table 9.3: Process Parameters for GNR and Si FET

The number of ribbons considered in the design of GNR-FET ring oscillator is 4, the oscillation frequency can be increased further by increasing the number of ribbons. Delay of GNR-FET based circuits decreases as we increase the number of ribbons, henceforth frequency of oscillation can be boost up by further increment of number of ribbons. Figure 9.7 shows the simulation result of frequency of 3 stage ring oscillator with variation in number of ribbons in FET and it can be concluded that GNR-FET with six ribbons results frequency of 15MHz which is significantly higher than frequency of Si-FET ring oscillator.

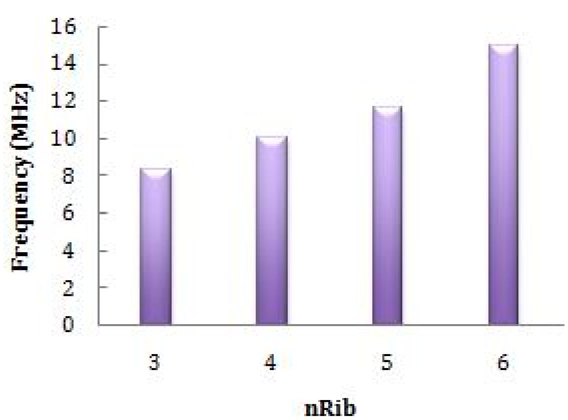

Figure 9.7: Frequency of oscillation with variation in number of ribbons

9.5 Variability Analysis of Graphene FET with Graphene Interconnect

Variability refers to the fluctuations in the parameters which affects the output performance of the entire design is affected. Thus in order to keep consideration for the varying performance it is necessary to perform variability analysis. Since in the previous section it has been observed that the system performs better with MLGNR used for both driver and interconnect in the DIL model, in this section we analyse the affect on the system when certain parameters are varied. The output parameters considered are delay and power dissipation.

For this analysis parameters for both interconnect and transistor are considered to vary with 10 percent variation. In Figure 9.8 it can be seen that the mean delay and mean power dissipation has been calculated for different interconnect lengths ranging from 0.5 to 3 mm using Monte Carlo methodology. The R, L and C are considered as the varying parameters and total number of sample for each interconnect length is taken as 1000.

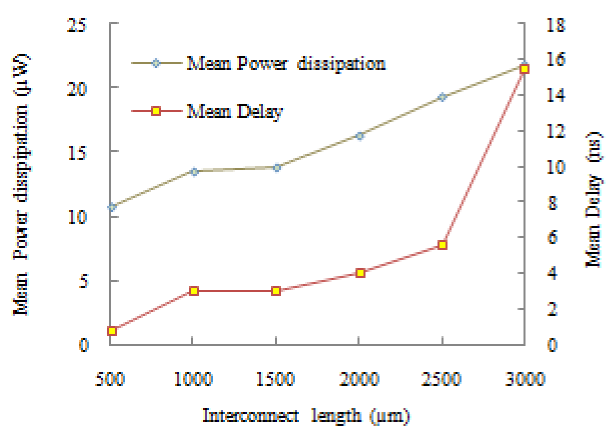

Figure 9.8: Performance analysis for variation in MLGNR interconnect parasitics

Further the variability of graphene FET is analysed for varying oxide thickness and number of MLGNR ribbons. This can be observed in Figure.9.9 where the oxide thickness is varied with 4 percent and corresponding delay and power dissipation are calculated.

Further the effect of number of ribbons on output performance is observed in Figure 9.10 Due to the increase in number of ribbons the width of the driving transistor is also increased thereby depicting the output variation with respect to

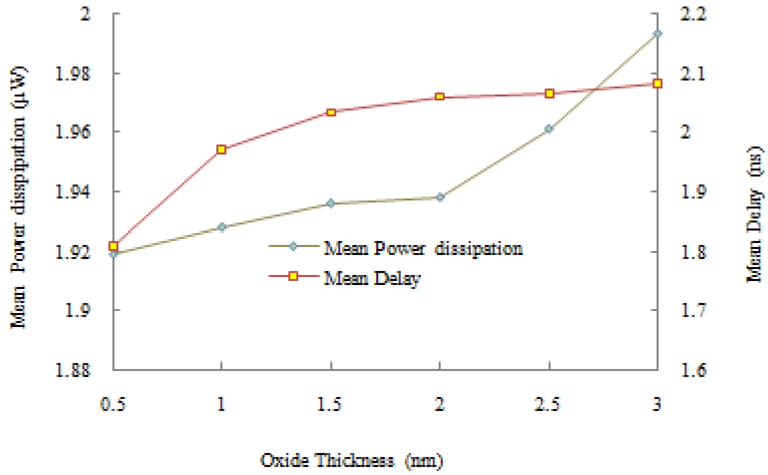

Figure 9.9: Performance analysis for variation in oxide thickness

varying CMOS width.

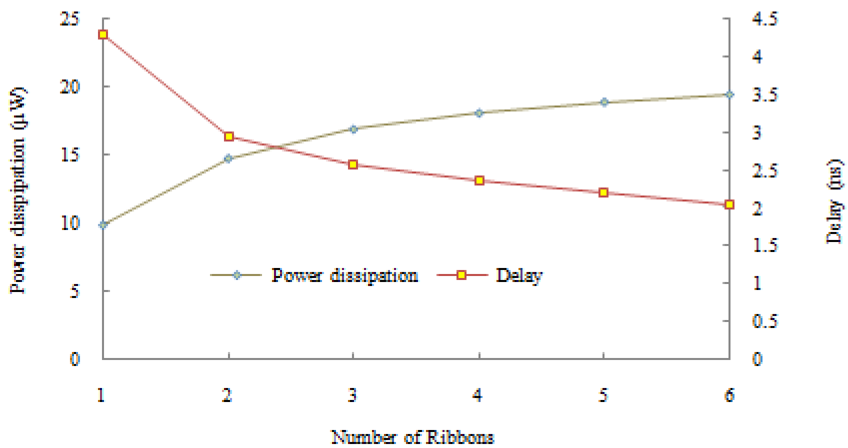

Figure 9.10: Performance analysis for variation in number of ribbons

Figure. 9.11. represents the output performance due to variation in dielectric constant. The power dissipated and delay are observed with respect to the constant being varied from 4 to 20.

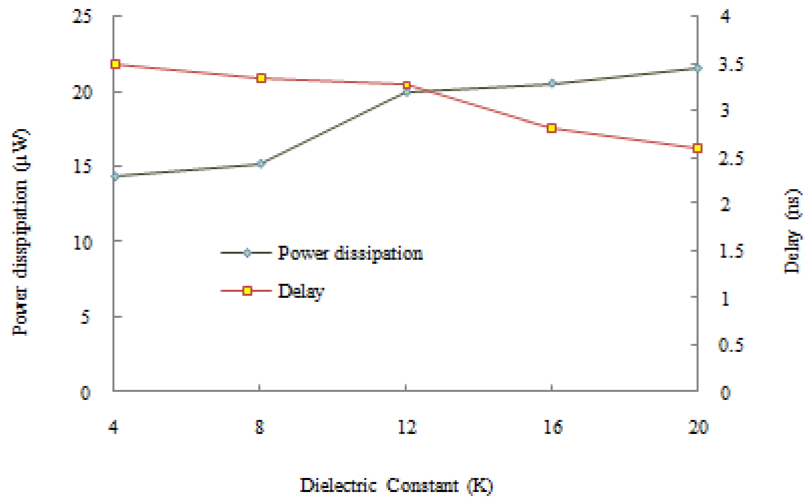

Figure 9.11: Performance analysis for variation of dielectric constant

CHAPTER 10
Conclusion

- The proposed technique employs an inverter load in the DIL model employed for the mathematical analysis. The transistor is modeled using nth power law for different region of operations. Performance of copper and MLGNR have been compared using the simulation and FDTD method. Performance comparision is based on power dissipation and delay. It is observed that the MLGNR interconnect gives better performance compared to the commonly used interconnect material. Further the proposed FDTD method is compared with the simulation result for transient analysis. It is observed that the technique and the conventional method gives an error of 1.8 percent which is very close to the simulation results. Thus it can be inferred that the proposed FDTD technique with CMOS load can be used to model the interconnects in VLSI design.

- To make the analytical model more robust and stable. US-FDTD is proposed for the DIL model. US-FDTD is not limited to Courant condition as in the case of FDTD thereby making it more practical for longer interconnects. The results are validated using HSPICE simulation results. The average percentage error is observed to be less than 1percent for the estimation of crosstalk induced performance parameters. Moreover, it is observed that the proposed model is highly time efficient than the conventional FDTD model.

- Neural Network (NN) is an advanced machine learning technique which has been rarely investigated and employed for analysis of on-chip interconnects. The current research work utilizes the prospective NN technique for faster and accurate prediction of system comprising of DIL model. The proposed method takes into account different on-chip interconnect lengths and thus varying parasitics in order to analyze the performance parameters viz. delay and power dissipation. The proposed method is validated and tested for different datasets. The parameter considered for validation is mean square error (MSE). Further, results of the proposed NN based model are compared with the SPICE simulation results. It is observed that error is less than 5 percent for all test cases, thereby providing highly accurate results. Also, comparison based on the computational time requirement is performed. It is envisaged that the proposed NN based design is nearly 5 times faster than conventional method. Hence, the NN based model gives a considerable advantage when large dataset is considered. This also enables to save considerable computational effort and is highly beneficial for circuits with large number of active and passive components embedded in VLSI integrated circuit designs. The neural network is therefore a well suited technique that is fast, robust and dynamic in nature and can be effectively applied for designing and performance evaluation of VLSI systems.

- The proposed system is aimed to design an accurate NN with high regression coefficient and minimum mean square error. This design is trained, validated and tested with HSPICE dataset. After the accuracy of the network is checked, the optimum aspect ratio is predicted using the performance parameters that are delay, power dissipation and loading. For the optimized designing of the system using NN, it is envisaged that the obtained values are very accurate and percentage error is less than 2 percent compared to the actual values. The constructed NN model is also utilized to evaluate the output performance of the DIL system. . It is investigated that the performance gain in terms of computation is nearly five times over HSPICE model. From the several analyses presented in the research, it can be strappingly inferred that novel neural network approach is efficient for optimized designing and accurate performance evaluation of DIL system.

- The approach incorporates a systematic process comprising of creation of initial data set, then training and building the NN based model. This is followed by testing of the model. The developed neural network based model is computationally efficient. The validity and accuracy of developed model is ensured using regression plots and analyzing mean square error. Further, variability analysis have been performed using NN based model. This has also been validated using conventional Monte Carlo method. It is analyzed that NN based model is 9.2 times faster as compared to Monte Carlo method. Since neural network does not have a-prior knowledge, it has the capacity to grasp from abstract dataset and thereby it is not limited to a particular interconnect dimension. Also the proposed model can handle high dimension dataset which have unknown non-linear relationship with each other. The neural network based model is versatile, dynamic and can be effectively incorporated to implement, analyze and design efficient circuits and systems.

- The comparision using different permutations of silicon and graphene with FET and interconnects displays graphene FET with graphene interconnect as a comparatively better DIL model. The comparision is based on performance parameter namely delay and power dissipation. Further graphene FET shows higher frequency in a ring oscillator compared to Si-FET. Also it is observed that on increasing the ribbons of MLGNR the frequency of operation increases. Thus it shows that graphene interconnect and FET can be a prospective alternative to the current DIL models. Variability analysis has also been performed for the proposed DIL model

CHAPTER 11

List of Publications

- Ajita Misra, Yash Agrawal, Vinay Palaparthy and Rutu Parekh "Variability Analysis of On-Chip Interconnect System using Prospective Neural Network", Springer International Conference on Advances in VLSI and Embedded System (AVES-2019), SVNIT Surat.

- Ajita Misra, Diksha, Yash Agrawal and Vinay Palaparthy "Performance Evaluation of On-chip Interconnect System using Prospective Neural Network Design," 2020 IEEE International Students' Conference on Electrical, Electronics and Computer Science, MANIT Bhopal.

- Ajita Misra , Yash Agrawal , Vinay Palaparthy and Bakul Gohel "Novel Neural Network Based Optimized Designing and Performance Evaluation of On-Chip Interconnect System in Integrated Circuits" (to be submitted).

- Ajita Misra, Yash Agrawal, Vinay Palaparthy and Rutu Parekh "Accurate FDTD Model Formulation and Prominent Neural Network based Optimized MLGNR Interconnect System Designing with Incorporation of Practical Driver and Receiver " (to be submitted)

- Ajita Misra, Diksha, Yash Agrawal and Vinay Palaparthy "Performance Analysis of Graphene Interconnects with Graphene MOSFET" (to be submitted)

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