1V Rail to Rail Operational Amplifier Design for Sample & Hold Circuits

by

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Declaration

This is to certify that

(i) The thesis comprises my original work towards the degree of Master of Technology in Information and Communication Technology at DA-IICT and has not been submitted elsewhere for a degree,

(ii) Due acknowledgement has been made in the text to all other material used.

(Mahesh Kumar Dilwani)

Certificate

This is to certify that the thesis work entitled "*1V Rail to Rail Operational Amplifier Design for Sample & Hold Circuits*" has been carried out by *Mahesh Kumar (200711004)* for the degree of Master of Technology in Information and Communication Technology at this Institute under my supervision.

Prof. Chetan Parikh

(Thesis Supervisor)

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Table of Contents

Abstract

At low voltage, the input common mode voltage of Operational amplifier is limited which restricts its use as a buffer. This works deals with designing a rail to rail amplifier. The Thesis presents a 1V rail to rail operational amplifier that has been used as a unity gain buffer in the sample and hold circuit for 1V 10 bit 1MSPS pipeline ADC in 0.18µm technology. The Operational amplifier is designed using dynamic level shifting technique which uses an additional input CM adapter circuit for fixing the input common mode voltage. Novelty in the input CM adapter circuit and a low value of gm fluctuation (±0.245%) has been achieved. The Operational amplifier is implemented in standard CMOS technology.

An open loop architecture is chosen for the implementation of sample and hold circuit. The transmission gate switch is used in the sample and hold circuit for reducing the effect of channel charge injection and clock feedthrough. Also, the transmission gate switch offers a low resistance as compared to pMOS or nMOS switches. The sample and hold circuit speed up to 1MSPS has been achieved.

List of Principal Symbols and Acronyms

μ	Mobility of charge carrier
β	Device transconductance
W/L	Width / Length of Transistor
C	Capacitance
g_m	Transconductance
A	Open loop gain
R	Resistance
I	Current
ro	Output Resistance
k	Boltzmann's constant
Z	Impedance
P	Pole
Mx	Transistor
V	Voltage
pMOS	p channel MOSFETs
nMOS	n channel MOSFETs
VDD	Supply
GND	Ground
Vt	Threshold voltage
Vref	Reference voltage
Vi+, Vi-	Input Voltage Signals
Vi,cm	CM Adapter Input common mode voltage
Vi,dm	CM Adapter Input differential mode voltage
Vip,cm	CM Adapter Output common mode voltage
Vip,dm	CM Adapter Output differential mode voltage
CM	Common Mode
DM	Differential Mode
LG	Loop Gain
SR	Slew Rate
PM	Phase Margin
UGB	Unity Gain Bandwidth

LGBW	Loop Gain Bandwidth
CMRR	Common Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio
ICMR	Input Common Mode Range
OCMR	Output Common Mode Range

List of Tables

List of Figures

Chapter 1
Introduction

1.1 General

In this era of System on Chip Design, the analog sub blocks need to be integrated with the digital subsystems which impose challenges in the design of analog circuits in a typical digital CMOS process. Also, the low power consumption requirements of digital subsystem demand the analog circuits to be designed at low voltages. There are several other reasons for designing the analog circuits at low voltages which are listed below: [17]

1) As the channel length is shrinking, the density of components is increasing on a single chip but silicon chip can only dissipate a limited amount of power per unit area. To overcome this, power per function in the chip has to be down so the supply voltage has to be reduced in order to prevent overheating.
2) The Gate oxide thickness has become several nanometres thick due to channel length downscaling so, in order to ensure device reliability the supply voltage has to be reduced.
3) In order to have a longer battery life in a battery operated system, both the supply power and the supply voltage has to go down.

1.2 Motivation

Sample and Hold circuits are heart of any Analog to Digital Converter and is used to improve the dynamic performance of the ADCs. Unity gain buffers are used to implement sample and hold circuits. With the increasing demand for the low power battery operated systems, the unity gain buffers need to be designed at low supply voltage but the voltage headroom available is limited at low supply voltages so noise starts dominating over the signal thereby reducing signal-to-noise ratio (SNR) as well as the dynamic range of the sample and hold circuits. At higher supply, this is not a problem because the signal range is high as compared to noise. Therefore, to improve SNR rail to rail signal swing is required at the input as well as at the output of unity gain buffer at low voltages.

1.3 Organisation of the Thesis

Chapter 2: This chapter mainly focuses on the literature survey on the Operational amplifier design techniques. Different design techniques are compared and their basic functionality is discussed.

Chapter 3: This chapter deals with the design and implementation of complete Operational amplifier. Novelty in the design of Operational amplifier is presented. Also, the sample and hold circuit design issues and its implementation issues are discussed.

Chapter 4: This chapter covers the simulation results. The specification of Operational amplifier and the Sample & Hold is mentioned and practical results have been shown.

Chapter 5: Here conclusion and future work is discussed.

Chapter 2

Literature Survey

2.1 Rail to Rail Operational Amplifier Design Techniques:

There are different design techniques available in the literature for performing rail to rail operation. One outweighs the other in terms of their performance. These techniques are as follows:

1) Complementary pair
2) Double n or p pair
3) Bulk driven Transistors (Back Gate Transistors)
4) Multiple input Floating Gate (MIFG)Transistors
5) Low Threshold (Vt) Transistors
6) On chip voltage Multiplication

2.1.1 Complementary pair

This is the most conventional design technique used for achieving rail to rail input/ output swing. In this, a p channel differential pair is placed in parallel with the n channel differential pair so that it works for the whole input common mode voltage range (i.e., from GND to VDD) as shown in Fig.2.1.1a but the gm vary as input common mode vary near the middle of the supply due to the overlapping of their transition regions where both n and p channel differential pairs works simultaneously as shown in Fig.2.1.1b.

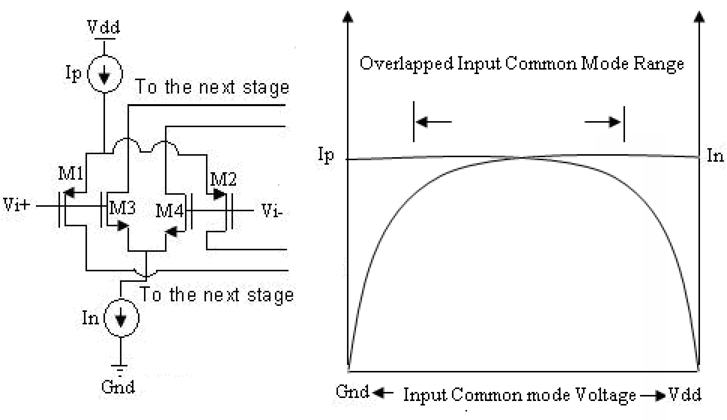


Fig.2.1.1a: Complementary pair showing the overlapped transition region [17]

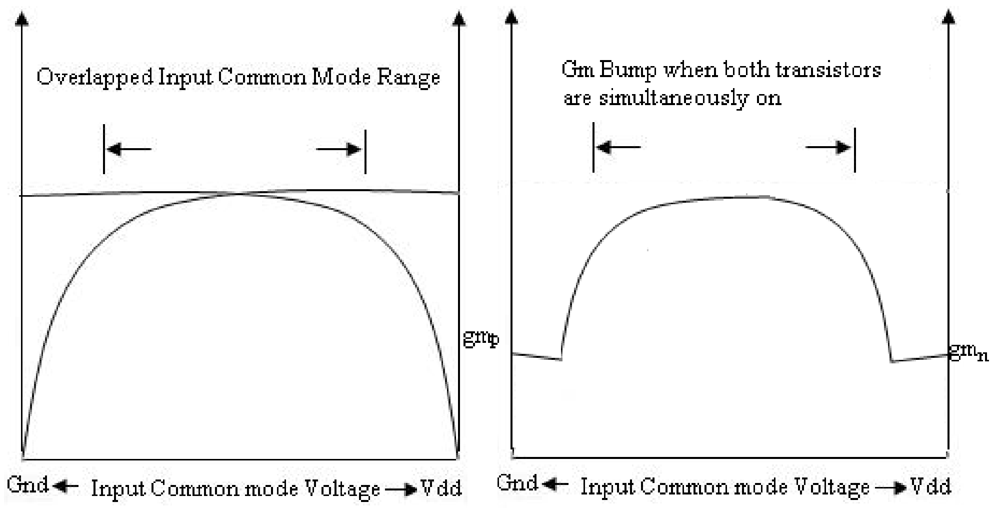


Fig.2.1.1b: Variation of gm as the input common mode voltage is varied [17]

There are certain disadvantages of using complementary pair which are as follows:

1) The complementary pair suffers from the problem of matching between the mobility of electrons (majority carriers in nMOS transistors) and holes (majority carriers in pMOS transistors). Generally, the mobility of electrons is 2-3 times the mobility of holes so (W/L) of p channel differential pair has to increase to make their β's equal which increases the input capacitance. The expressions for βn and βp can be written as:

$$\beta n = \mu n \; Cox \; (W/L)n$$

$$\beta p = \mu p \; Cox \; (W/L)p$$

2) In order to obtain constant transconductance, the g_m of the n channel differential pair must precisely match with that of p channel differential pair which is difficult to realize in a given process variation in standard CMOS technology.
3) A common drawback in all the complementary schemes available in the literature is the signal dependent input referred offset voltage. Usually, n or p pairs have different offsets due to random process variations so effective input referred offset depends upon whether n or p differential pair is active. This offset introduces large distortions.
4) The total g_m fluctuation using complementary pair varies between ±1.5% to ± 10% which degrades the ac performance.

5) Complex circuitry is required to obtain constant g_m when both n and p channel differential pair works simultaneously.

2.1.2 Double n or p pair:

This technique uses two identical differential pair instead of using complementary pair. The primary difference between the complementary and the double n or p pair technique is that it uses feedforward cancellation to make gm constant rather than overlapping the transition regions of input differential pairs. Fig.2.1.2a below shows one such rail to rail input stage implemented using two identical n channel differential pair. Here the input signal is applied to one n channel differential pair while the level shifted input to the other identical n channel differential pair so that rail to rail operation is performed.

This technique also has its own merits and demerits:

1) This technique does not require strict matching of the input devices and hence no compensation is needed for the difference in the mobility of electrons and holes.
2) Overall gm fluctuation as low as ±0.5% has been achieved using this technique.

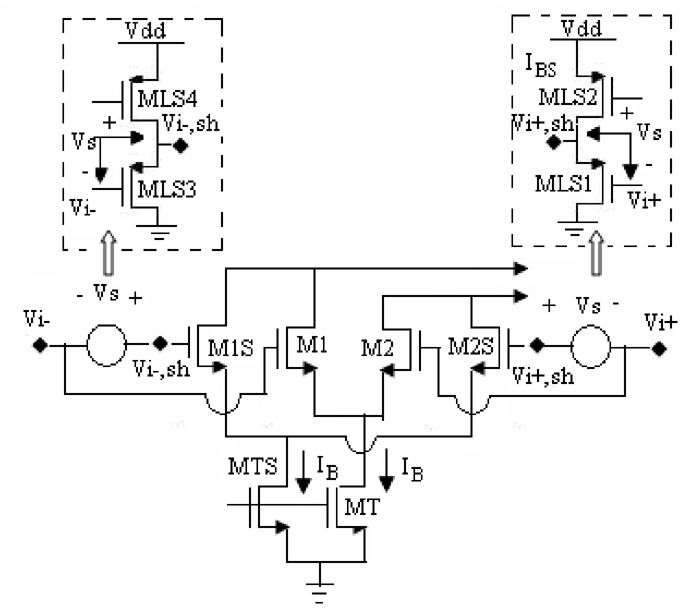


Fig.2.1.2a: Rail to Rail input stage based on two n channel differential pair [7]

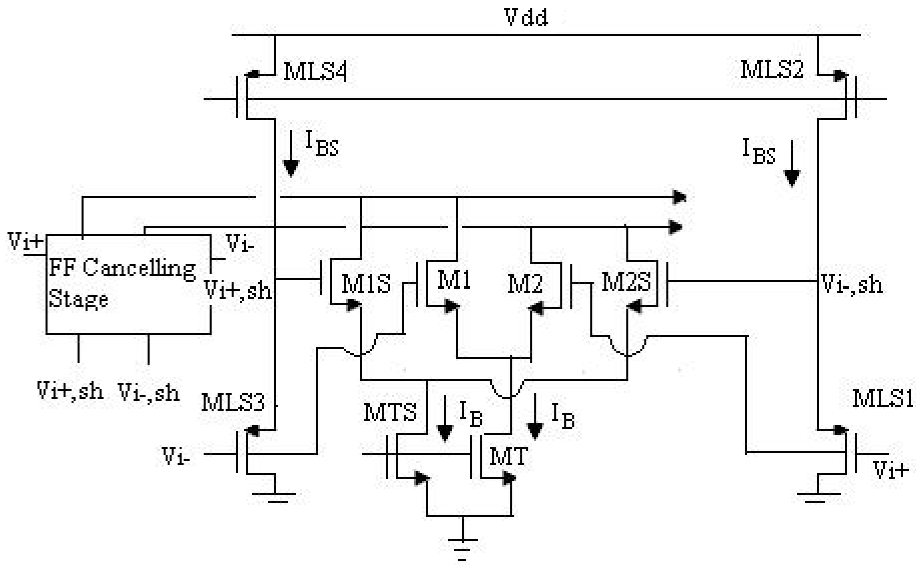


Fig.2.1.2b: Rail to Rail input stage with feedforward cancelling stage [7]

3) This technique is valid for any gm versus Id characteristics of the amplifier input transistors and hence is compatible with the modern sub micrometer CMOS devices in which the voltage-to-current square law in the saturation region is not completely satisfied.
4) It requires strict matching between the amplification transistors and the input level sensing transistors in the feedforward cancelling stage internal circuitry as shown in Fig.2.1.2b to exactly cancel the effect of gm variation when both n channel identical pairs works.
5) Additional biasing circuitry and complex circuits are required to counteract with the g_m variation when the input common mode voltage vary near the middle of the supply voltages which increases the power consumption of the amplifier.

2.1.3. Bulk Driven Transistors

In Bulk driven transistor technique, the input is applied to the bulk terminal rather than at the gate of the input transistors thereby removing any constraints on the threshold voltage which is the key problem at low voltages e.g.1V. Now, it is not necessary to spend a part of the input voltage in turning on the transistors. Fig.2.13a shows one such bulk driven and its counterpart gate driven configuration.

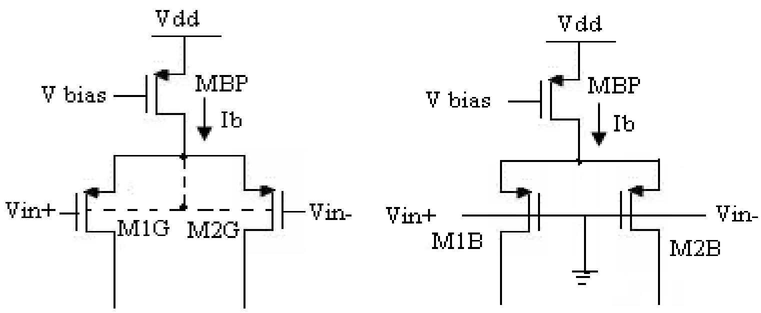


Fig.2.1.3a: Gate driven and Bulk driven differential input stage [10]

Bulk driven Transistors have the following properties:

1) Bulk driven input transistors have big input capacitances.
2) Bulk driven input transistors have lower transconductance as compared to that of gate driven. The transconductance of bulk driven transistors are generally 4-5 times less than that of gate driven in standard CMOS as shown in Fig.2.1.3b.The reduction of input transconductance along with the increase in the input capacitance leads to decrease in ft (transition frequency) which limits the maximum achievable frequency of the circuit using these devices.

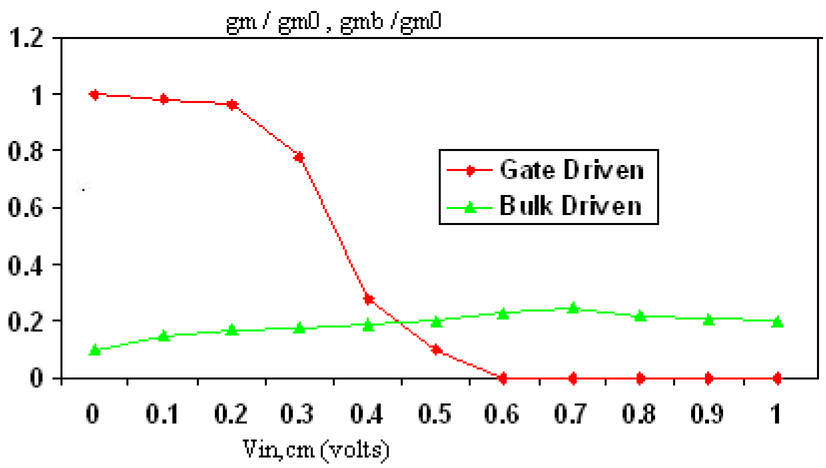


Fig.2.1.3b: gm relationship between Gate driven and Bulk driven Transistors [10]

3) Input referred noise in these transistors is increased due to the reduction of the intrinsic gain of the bulk driven transistors.

4) The physical implementation of bulk-driven MOS transistors includes a parasitic bipolar junction transistors but that does not lead to latch up provided that the value of the forward current through the bulk terminal is maintained at a low level and the layout of the circuit is carefully drawn.
5) Bulk driven transistors give bad ac performance due to lower transconductance and big input capacitance.
6) This technique can't be used where both n and p transistors are required to be bulk driven for a given process that is for an n – well process there is only a p bulk driven mosfets are available.

2.1.4 Multiple Input Floating Gate Transistors

Multiple Input Floating Gate (MIFG) Transistors make use of a capacitive division at the input of the transistor to attenuate the signal before it is processed by the amplifier employing single input differential pair such that it lies in the common mode input range of the single input differential pair. Fig.2.1.4 shows the capacitive division done at the input of transistor M1 by capacitors C1 and C2 where V_{input} and $V_{feedback}$ are the input voltage and feedback voltage respectively. V_{out} is the level shifted output applied to single input differential pair.

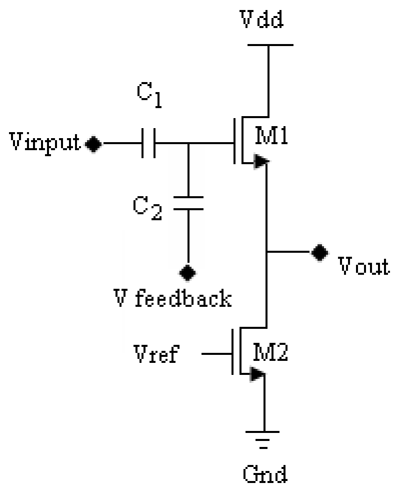


Fig.2.1.4: MIFG Transistors showing capacitive division at the input [17]

This technique has its own merits and demerits which are as follows:

1) This technique is based on dynamically shifting the input common mode of the input signal to the input common mode range of the single differential pair so only a single differential pair is required for rail to rail operation hence there is no mismatch problems like mobility mismatch and other problems which are associated with complementary pair and double n or p pair.
2) The MIFG transistors demand a special technology for their implementation which increases its cost of implementation.
3) Gm fluctuation as low as ±0.2% has been achieved using this technique [12].
4) The MIFG transistors have large capacitors connected to the input so they greatly load the previous stage and create an extra pole in closed loop configuration.
5) The gate leakage current in MIFG transistors increases as the technology downscales.
6) The ratio of MIFG capacitors is chosen in such a way that the input signal is attenuated enough to lie in the input common mode range of the amplifier and this ratio is usually set to around five or six which badly affect the gain bandwidth product (GBW) as well as noise response of the amplifier.

2.1.5 On Chip Voltage Multiplier

At low supply voltage a problem of dead zone as shown in Fig.2.1.5 occurs where the input differential pair(s) is (are) not working. This problem can be overcome by supplying some multiplied version of the input signal to the input differential pair(s) through on chip voltage multipliers but this technique is not robust in terms of technology downscaling and hence is usually avoided.

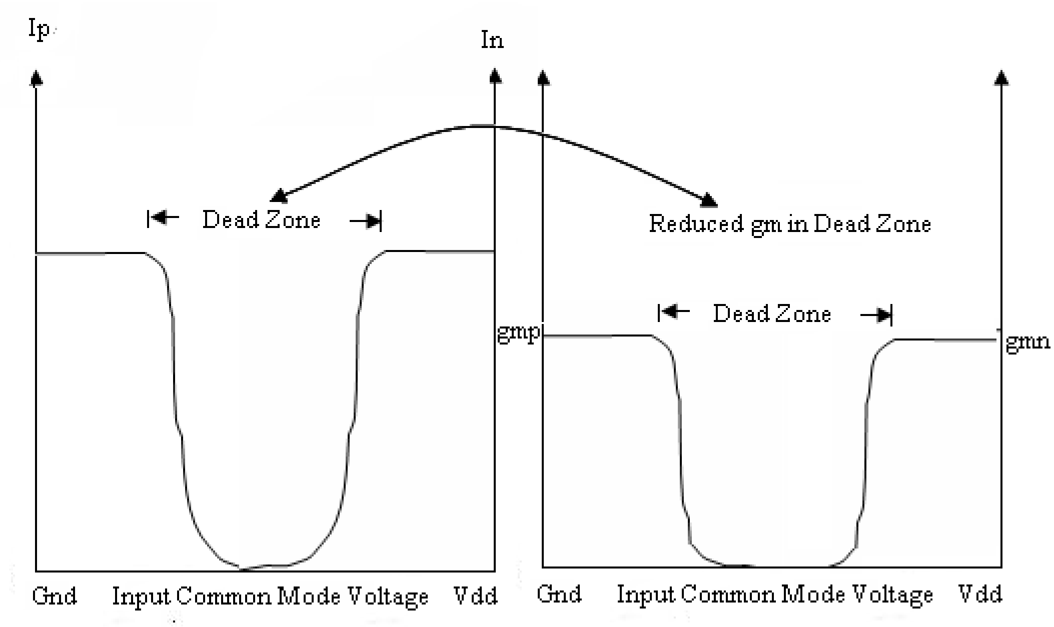


Fig.2.1.5 shows problem of dead zone in complementary pair at low voltages [17]

2.1.6 Low Vt Transistors

Low Vt Transistors are used where the high speed with low power consumption is one of the design requirement. In this, the transistors in the critical path from input to output terminals in a given circuit configuration have low threshold voltage while others have threshold voltage according to the technology used. Therefore, the transistors in the critical path have more overdrive than other transistors in the given circuit which implies greater speed can be achieved while having low power consumption but this technique is not robust with the technology downscaling as it causes serious problems due to the leakage current its cost of implementation is also very high.[17]

2.2 Architecture chosen for implementation

The proposed technique uses an extra input common mode (CM) adapter circuit placed before the actual amplifier having a limited input common mode voltage & implemented using single differential pair.

The task of this extra circuit is to dynamically shift the input common mode voltage to a fixed voltage which lies well inside the input common mode voltage range of the actual amplifier without affecting or attenuating the input differential voltage signal so that differential action of the actual amplifier remains unaffected.

The Input CM adapter circuit consists of a feedback amplifier which is responsible for fixing the input common mode voltage to a fixed reference voltage Vref through the action of negative feedback without affecting the input differential signal.

2.2.1 Comparison with the Existing Techniques

This Technique uses a single differential pair therefore the problems related to the complementary as well as double n or p pair is removed.

As the input transistors are gate driven so this prove to be better than bulk driven transistor technique in terms of ac performance.

Also, this technique is implemented in standard CMOS technology which reduces its cost of implementation therefore it overcomes the problem with the MIFG transistors, On chip voltage multiplier and low Vt transistors.

The next section shows the conceptual as well as transistor level implementation of the proposed technique. Also, the issues with the loop stability are discussed. The entire amplifier comprises input CM adapter circuit and amplifier implemented using single differential pair in two stages.

Chapter3

Operational Amplifier Design & Implementation

The design of complete Operational amplifier is divided into two parts:

1) Input CM Adapter Circuit Design
2) Two Stage pMOS Folded Cascode Amplifier Design

3.1. Input CM Adapter Design

3.1.1 Conceptual Design

The conceptual circuit schematic of input CM adapter is shown in Fig.3.1.1. It basically consists of a feedback amplifier, voltage controlled current sources and resistors connected in a feedback loop for sensing the input common mode voltage and fixing it to a reference voltage Vref.

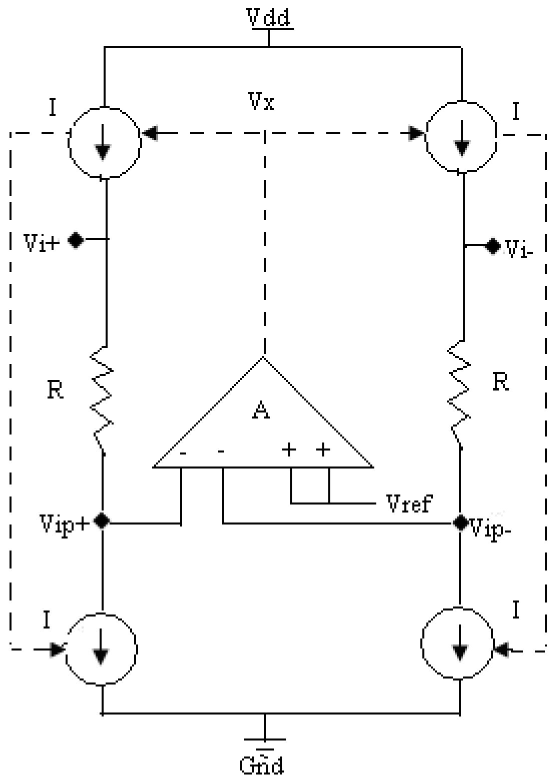


Fig.3.1.1 Conceptual circuit schematic for illustrating the operating principle of proposed input CM adapter [12]

In Fig.3.1.1, Vi+ and Vi- are the input voltage signals whose input common mode voltages vary rail to rail. Vip+ and Vip- are the corresponding CM adapter output voltage signals shifted by an equal amount –I*R which are also the negative input and output voltage signals of the feedback loop in CM adapter circuit. The value of current source I is controlled by the voltage Vx of a feedback amplifier. The CM adapter output common mode (Vip,cm)and differential mode voltage(Vip,dm) can then be expressed in terms of input common mode(Vi,cm) and differential mode(Vi,dm) voltage as:

For Vip,cm:

$$Vip,cm = Vref + \left(\frac{\mathrm{Vi,cm}}{\mathrm{Gm*2*A*R}}\right) \qquad \text{------------------(1)}$$

For Vip,dm:

$$Vip,dm = Vi,dm \qquad \text{--------------------(2)}$$

Equation (1) gives the direct relationship between the input and output common mode signal. Therefore, the CM adapter output common mode voltage is approximately equal to the reference voltage and it is attenuated by the open loop gain while the output and input DM component remains equal. Here the advantage of negative feedback is that it attenuates only the input common mode voltage while input DM voltage remains unchanged under perfect matching conditions.

3.1.1a Working of Feedback Loop:

Initially, as the input common mode voltage (Vi,cm) increases above Vref, the voltage Vip,cm also increases which is then applied to feedback amplifier having open loop gain A. The output voltage of feedback amplifier Vx thus decreases thereby increasing the current through the resistors which finally decreases the output voltage. Therefore the negative feedback action nullifies the effect of any variation in input common mode voltage and causes the output common mode voltage to be approximately to be equal to the fixed reference voltage Vref. But for Vi,cm less than Vref no current flow in the resistors and the feedback loop is opened.

3.1.2 Transistor Level Implementation

The Transistor level implementation of conceptual design uses a pseudo differential structure using transistors from M1-M6 along with the bias current sources M7-M8 for the implementation of the feedback amplifier as shown in Fig.3.1.2. The output of the feedback amplifier controls the current sources implemented using transistors M10 – M13. M14 has been included to make the drain voltage of M15-M12 and M15-M13 equal which minimizes the error due to finite output resistance. As the pMOS input differential pair is used, a low value of Vref (≈ 0.2 V) must be chosen.

For Vi,cm greater than Vref, the Vip,cm is fixed to a Vref but when the input common mode voltage falls below Vref no current flow in the feedback loop because the dependent current sources M10-M13 are off due to insufficient gate drive so the feedback loop is opened and Vip,cm will exactly follow Vi,cm.

For Vi,cm less than Vref, the current must flow through the resistors from Vip,cm to Vi,cm to close the feedback loop so that Vip,cm should remain tied to Vref for the whole input common mode range. The circuit which implements this is proposed in the next sub section.

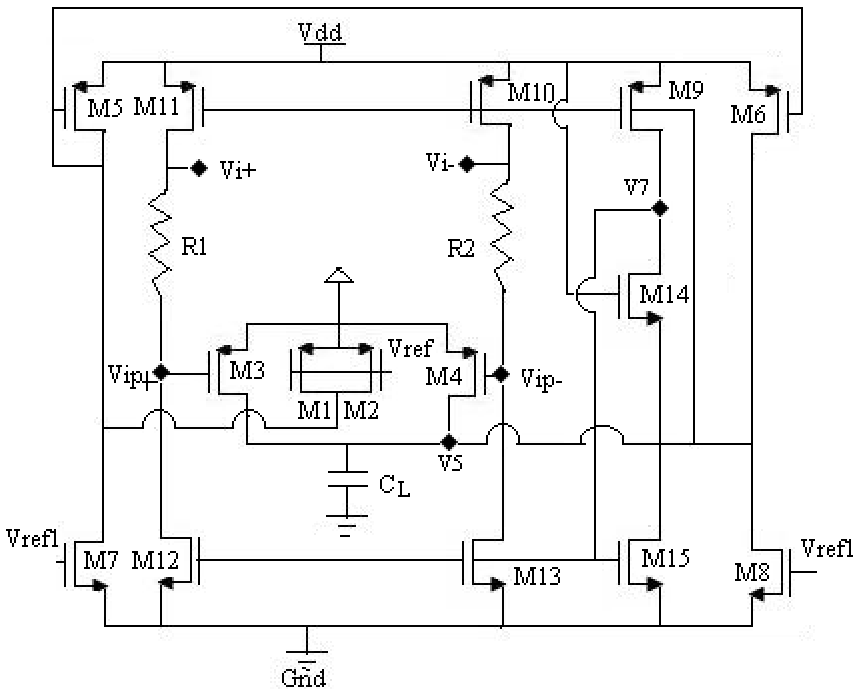


Fig.3.1.2: Transistor Level Implementation of Input CM Adapter Circuit

Following are the equations used for designing Input CM Adapter Circuit:

$$A = gm.rout$$

$$po = (\frac{1}{rout * CL})$$

$$V5 = \left(A * (Vref - (Vip + + \ Vip -)\ )\right)$$

$$I = -Gm * V5$$

$$Vip = Vi - (I * R)$$

$$\mathrm{Vip, cm} \ = \mathrm{Vref} \ + \ \left(\frac{\mathrm{Vi, cm}}{\mathrm{Gm} * 2 * \mathrm{A} * \mathrm{R}}\right)$$

$$Vip, dm \ = \ Vi, dm$$

3.1.3 Proposed Circuit for Rail to Rail Operation

The proposed circuit for getting rail to rail operation using input CM adapter circuit is shown in Fig.3.1.3. In this, two pairs of extra transistors ML1-ML2 and ML3-ML4 are used to make the current flow through the resistors to close the feedback loop. The idea behind this is to make transistor ML1-ML4 work only when the voltage dependent current source transistors M10-M13 are off.

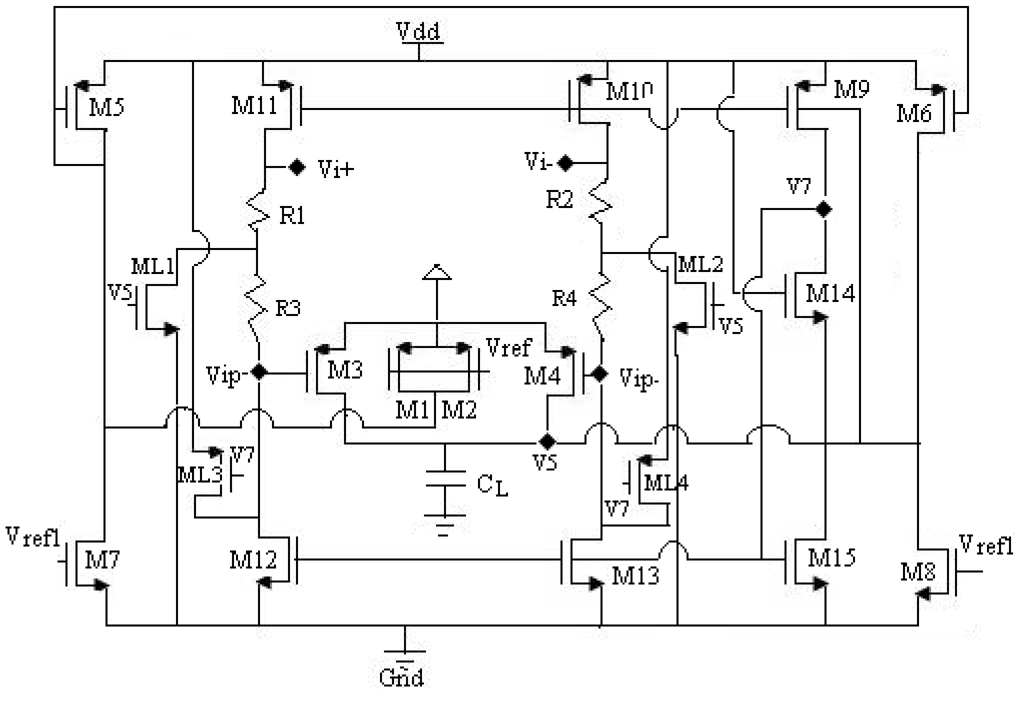


Fig.3.1.3 Proposed Circuit for rail to rail operation

When the input common mode voltage is lower than Vref, then the current sources are off because V5 and V7 are sufficiently high and low respectively but these are utilized to turn on ML1-ML2 and ML3-ML4 respectively at the same time. As soon as the input common mode voltage exceed Vref, the voltage V5 and V7 become low and high enough to turn on M10-M13 transistors and turn off the transistor ML1-ML4. Therefore, the circuit works in its usual manner for Vi,cm greater than Vref and extra transistor pairs come into action when Vi,cm becomes lower than Vref. The Transistor ML1-ML2 pair is designed to provide a low resistance path to ground.

The resistors used in the earlier circuit is modified and divided into two unequal half. A sufficiently high value of resistor R1, R2 is selected in order to avoid the current flow into the input node and a low value of resistors R3-R4 is used. In this way, the output voltage is fixed to Vref for the whole common mode range.

3.1.4 Loop Stability

The Input CM adapter circuit consists of an negative feedback loop so it's stability must be ensured for reliability of the circuit. The circuit for checking the loop stability is shown in Fig.3.1.4. In this, the input node is connected to an ac ground, the loop is opened and the ac input is applied to the feedback amplifier. The two pMOS and the two nMOS transistors used have the same aspect ratio respectively.

The entire loop consists of two poles one at the output node and other at the output of the feedback amplifier (assuming single pole model for the feedback amplifier). The loop gain can then be expressed as:

$$LG(s) = \frac{vo}{vi} = -\left(\frac{gm1*gm*rout}{R^{-1}+go2} * \left(\frac{1}{\left(1+\frac{s}{po}\right)*\left(1+\frac{s}{p1}\right)}\right)\right) \dots\dots\dots\dots\dots\dots\dots (8)$$

Where $A = gm * rout$

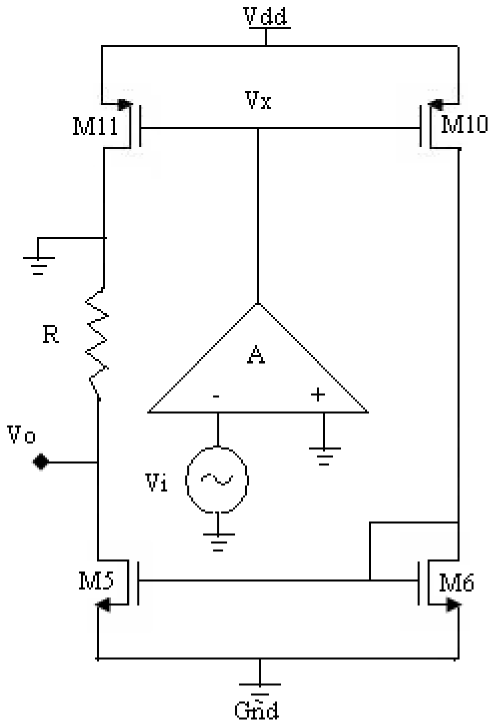


Fig.3.1.4 Equivalent CM circuit for stability analysis of feedback Loop

Dominant Pole $$po = \left(\frac{1}{rout * CL}\right)$$

Secondary pole at the output node vo

$$p1 = \left(\frac{R^{-1} + go2}{Cp}\right)$$

Cl →Load capacitor which also acts as a compensation capacitor.

Cp →Parasitic capacitance at the output node.

Loop gain bandwidth can be thus expressed as:

$$LGBW = \left(\frac{gm1 * gm}{(R^{-1} + go2) * CL}\right)$$

Therefore,

$$\frac{p1}{LGBW} = \left(\left(\frac{CL}{Cp}\right) * \left(\frac{(R^{-1} + go2)^2}{gm1 * gm}\right)\right) \dots\dots\dots..(9)$$

To get a reasonable phase margin the ratio $p1/LGBW$ must be above a certain value (i,e. above 1.5 for a phase margin of 60 degrees for a two pole system). Therefore, from equation (9) it can be concluded that feedback amplifier transconductance gm and the load capacitor CL must be kept low and high respectively in order to ensure that $p1$ lies far enough from the loop gain bandwidth.

3.2 Two Stage pMOS Amplifier Design

A low voltage pMOS folded cascode amplifier is shown in Fig.3.2 is implemented in two stages for achieving the gain and the output swing requirements

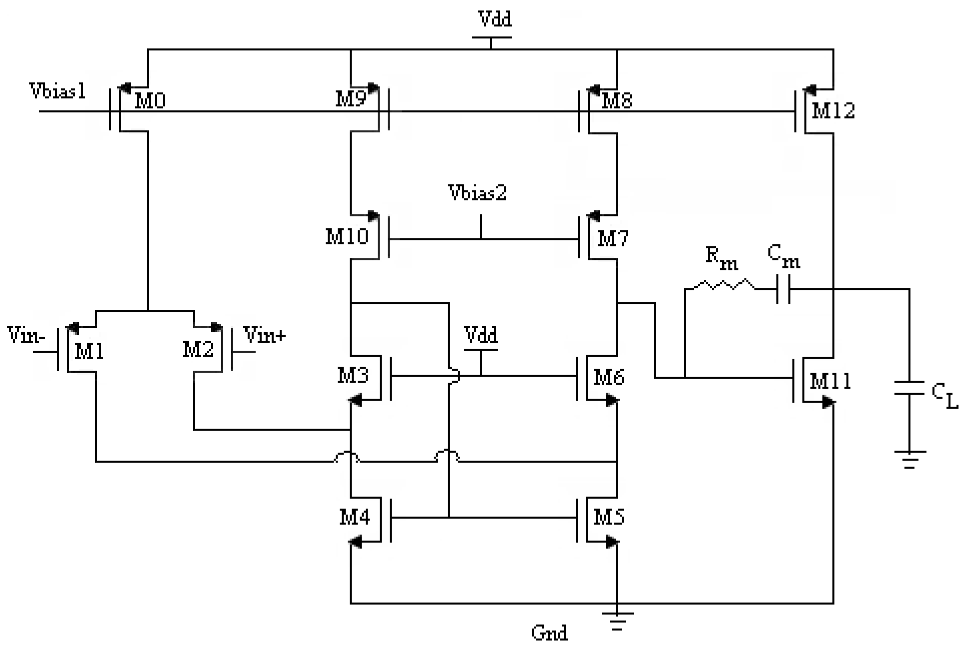


Fig.3.2 Two Stage pMOS Folded Cascode Amplifier Circuit

3.2.1First Stage Requirements:

The Tail current of the first stage is chosen to satisfy the gain, UGB and the Slew rate requirement. The current flowing in the cascode branch is 1.2 times the tail current source so that they are not turned off during slewing. The swing in the first stage is not important so greater overdrive voltage can be assigned in the cascode transistors which greatly reduces the transistor sizes. Also, the numbers of bias voltages used have been reduced so less bias voltages need to be generated. The *ro* of the transistor has been increased by taking length multiples to achieve higher gain.

3.2.2 Second Stage Requirements:

The second stage is responsible for providing the rail to rail output swing while providing a reasonable gain. A simple common source amplifier with an active pMOS load is used to implement the second stage. The miller resistor and miller capacitor are connected in between the outputs of first stage and the second stage to provide the reasonable phase margin. The value of load capacitor is determined from the connection of sample and hold circuit to the internal stage modules of pipeline ADC.

3.2.3 Design Equation used for Implementation:

$Gain\ A_{Folded} = [gm1{,}2\{(\mathrm{gm6ro6}\ (\mathrm{r05}||\mathrm{r01})||(\mathrm{gm7\ ro7r08})\}\mathrm{gm11}(\mathrm{ro11}||\mathrm{r012})]$

$Slew\ Rate\ SR = \frac{I_{Mo}}{C_m}$

$Unity\ Gain\ Bandwidth\ UGB = \frac{gm1{,}2}{C_m}$

$Maximum\ Input\ Common\ Mode\ range\ V_{ICMR(Max)} = Vdd - V_{DSATM0} - V_{SG1,2}$

$Minimum\ Input\ Common\ Mode\ range\ V_{ICMR(Min.)} = V_{DM1,2} - |VTPM1{,}2|$

3.3 Sample and Hold Circuit Design

A Simple open loop sample and hold architecture has been chosen as shown in Fig.3.3. It consists of a transmission gate switch Mn-Mp pair, sampling capacitor Ch and a unity gain buffer. Transmission gate switch instead of pass transistor switch is chosen to reduce the effect of channel charge injection and clock feedthrough. Vin and Vout are the input and output voltage signals of the sample and hold circuit and clock signal controls the transmission gate switch. The sample and hold circuit is designed for 1V 10-bit 1MSPS pipeline ADC.

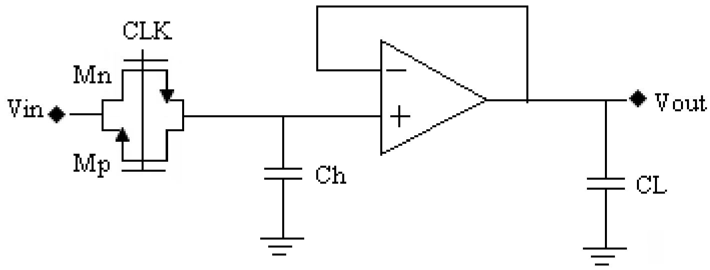


Fig.3.3 Open Loop Sample and Hold Circuit

3.3.1 Design Considerations:

3.3.1a Selection of Sampling Capacitor

The sampling capacitor plays an important role in deciding the signal to noise ratio (SNR) since in sample and hold circuit the maximum rms sampling noise is$\left(\frac{KT}{C_h}\right)$. So, a high value of sampling capacitor is desired in order to have a good SNR but high value of sampling capacitor means the sampling period will also become high thereby reducing the speed of the circuit. Thus an optimum value of capacitor is chosen which satisfy both the above requirements.

3.3.1b Selection of Transmission gate Resistance

Once the sampling capacitor value is determined, the transmission gate resistance (R_x) can be found out from the time constant specification. As this is a simple RC sampling circuit, the time constant(τ) can be written as:

$$\tau = R_x C_h$$

$$\mathrm{R_x} = \frac{\tau}{\mathrm{C_h}}$$

3.3.2 Buffer Design Requirements:

3.3.2a Slew Rate

Slew rate is determined from the ability to charge the load capacitor to the full scale voltage (Vpp) within the time allocated for slewing (Ts/8). As a rule of thumb, the time allocated for slewing should be ¼ of half the sampling period (Ts/8) Therefore, slew rate can be calculated as:

$$Slew\ Rate \geq (\frac{V_{pp}}{\frac{T_s}{8}})$$

$$\geq \frac{8 * V_{pp}}{T_s}$$

So, for Vpp =1volts and Ts = 1µs

$$Slew\ Rate \geq 8\ V/\mu s$$

3.3.2b Unity Gain Bandwidth

As the slewing time is Ts/8 so the remaining sampling time 3Ts/8 is used for the small signal settling. The settling time determines the unity gain bandwidth from the following formula:

$$Unity\ Gain\ Bandwidth\ UGB \geq \left(\frac{\ln(2^{N+1})}{2\pi\beta t_{settling}}\right)$$

For N= 10 bits, $t_{settling} = 375\ ns$

Therefore, $UGB \geq 3.23\ MHz$

Also, $UGB = gm1{,}2/(2\pi CL)$

This relation also gives the same UGB as derived using settling time constraint.

3.3.2c DC Gain

The DC gain is calculated on the basis of error allowed for sample and hold circuit for a given resolution. The error that can be tolerated for an N-bit ADC is expressed as:

$$error\ e_o < 2^{N+1}$$

N=10 gives

$$e_o < 2^{-11}$$

Now, The DC gain can be calculated using the formula below:

$$e_o = \left(\frac{1}{1 + A_o\beta}\right)$$

Therefore, $Open\ Loop\ Dc\ Gain\ A_o \geq 66.22\ dB$

3.3.2 Tail Current

The tail current is determined from the slew rate specification. Thus, for a given slew rate, tail current source can be determined as:

For $C_m = 0.8pF$,

$$\frac{I_{tail}}{C_m} \geq 8V/\mu s$$

Therefore,

$$I_{tail} \geq 6.4\ \mu A$$

Chapter 4
Simulation Results

The complete circuit has been simulated using 0.18µm BSIM 3v3.1 Model parameters in 0.18µm technology.

In the frequency response curve, the dashed line shows the phase curve while the solid line represents gain of the amplifier.

4.1 Input CM Adapter

4.1.1 Input CM Adapter Basic Parameters:

Table 4.1.1: Input CM Adapter basic parameters

Parameters	Notation Used	Units	Value
Reference Voltage	Vref	V	0.2
Input Signal	Vi,cm	V	0 – 1
Output Signal	Vip,cm	V	0.195-0.209
Resistors	R1, R2	kΩ	15
Load Capacitor	CL	pF	1.2

4.1.2 Feedback Amplifier:

Table 4.1.2: Specifications of designed feedback amplifier

Parameters	Notation used	Units	Value
Feedback Gain	A	dB	20.22
Output Resistance	Rout	kΩ	260.15
Load Capacitor	CL	pF	1.2
Dominant Pole	Po	KHz	554.35

4.1.3 Feedback Loop Stability:

Table 4.1.3: Specification of designed feedback loop

Parameters	**Notation used**	**Units**	**Value**
Loop Gain	LG	dB	20.66
Loop Gain Bandwidth	LGBW	MHz	4.95
Secondary Pole	P1	MHz	51.72
Phase Margin	PM	Degrees	73.8°
Transconductance	Gm	mA/V	5.04e-004
Parasitic Capacitance	Cp	fF	52

4.2.1Operational amplifier based on p channel differential pair

Table 4.2.1 Specifications of Operational amplifier based on p channel differential pair

Parameters	Notation Used	Units	Value
Process	-----	μm	0.18
Supply Voltage	Vdd	V	1
Gain	Ao	dB	75.4
Phase Margin	PM	degrees	110°
Unity Gain Bandwidth	UGB	MHz	38.8
Common Mode Rejection Ratio	CMRR	dB	79.4
Power Supply Rejection Ratio	PSRR	dB	58.5
Input Common Mode Range	ICMR	V	0-0.225
Output Common Mode Range	OCMR	V	0.046-0.97
Power Dissipation	PD	μW	361

4.2.2 Complete Operational Amplifier:

Table 4.2.2 Specifications of Complete rail to rail Operational amplifier

Parameters	Notation Used	Units	Value
Process	-----	µm	0.18
Supply Voltage	Vdd	V	1
Gain	Ao	dB	75.43
Slew Rate	SR	V/µs	23.1
Phase Margin	PM	degrees	58.5°
Unity Gain Bandwidth	UGB	MHz	30.3
Common Mode Rejection Ratio	CMRR	dB	108
Power Supply Rejection Ratio	PSRR	dB	58.5
Input Common Mode Range	ICMR	V	0-1
Output Common Mode Range	OCMR	V	0.046-0.97
Power Dissipation	PD	µW	455

4.3 Sample and Hold Circuit:

Table4.3 Specifications of the Sample and Hold Circuit

Parameter	**Notation Used**	**units**	**Value**
Resistance	R	kΩ	1.1
Hold Capacitor	Ch	pF	10
Sampling Speed	Fs	MHz	1
Input signal range	ISR	V	0-1
Output Signal Range	OSR	V	0.046-0.97

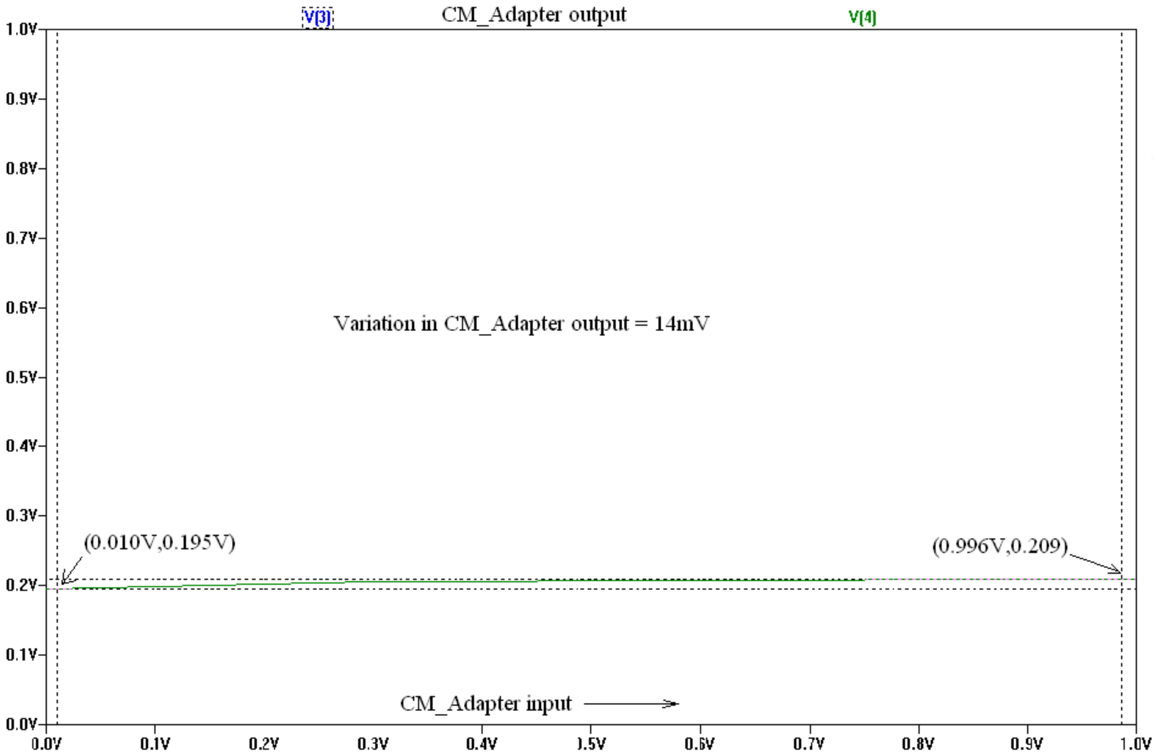


Fig.4.1 DC Characteristics of Input CM Adapter circuit

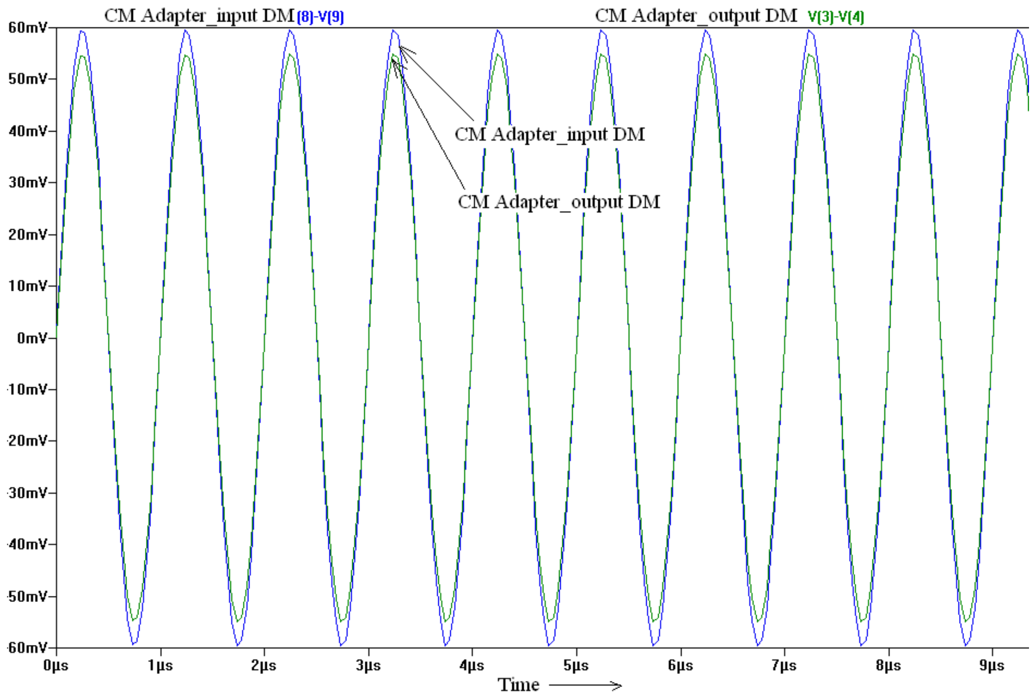


Fig.4.2 Input and Output DM component of Input CM Adapter circuit

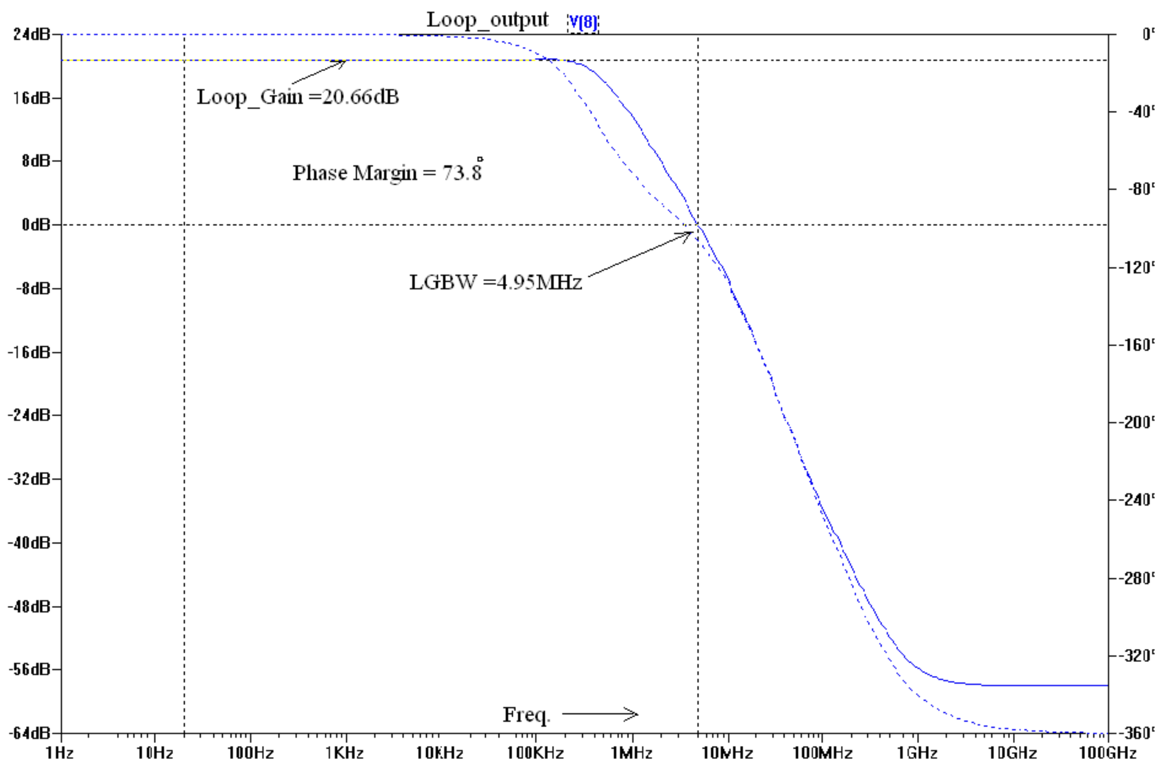


Fig. 4.3 Feedback loop stability analysis in Input CM Adapter circuit

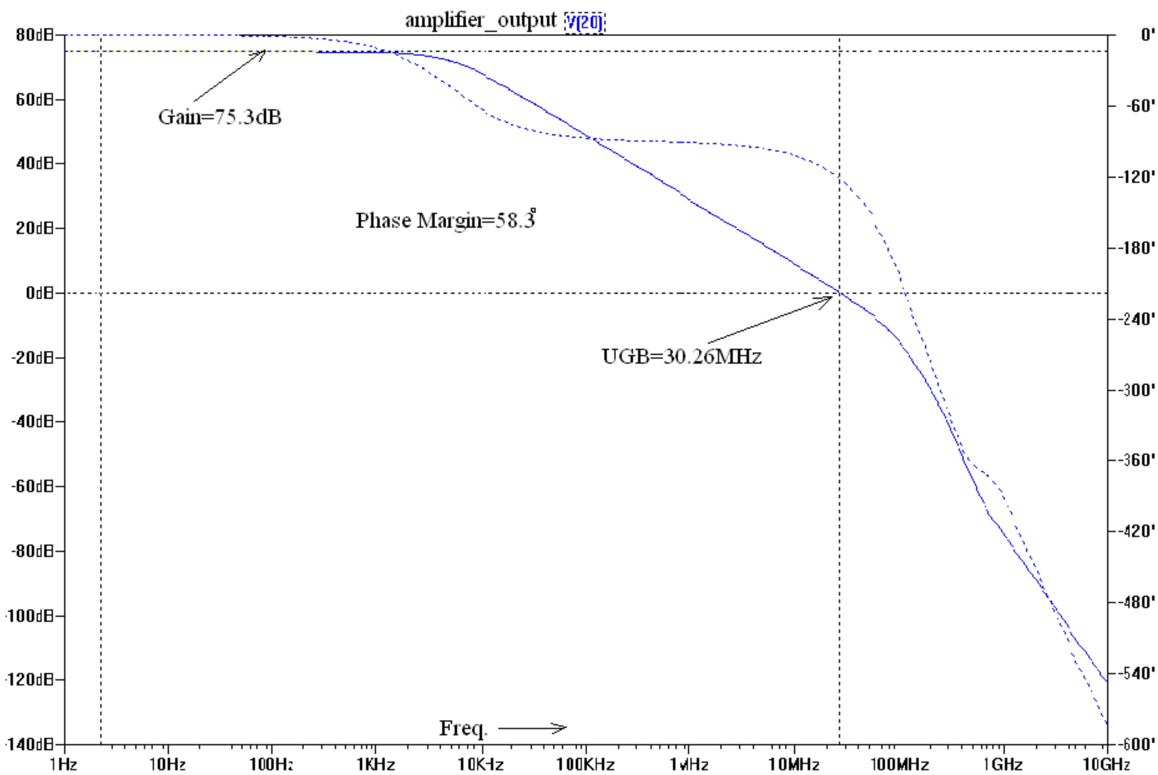


Fig.4.4 Frequency response of rail to rail Op-amp

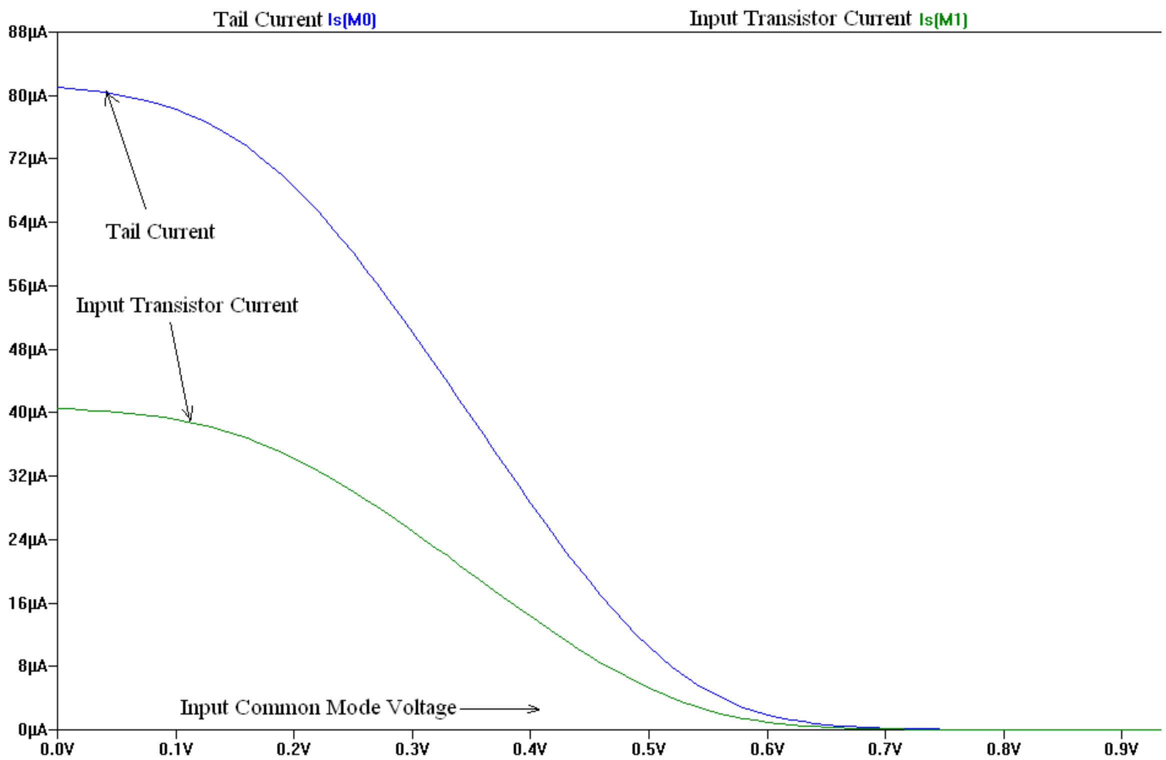


Fig.4.5 Input common mode range of a p channel input differential pair

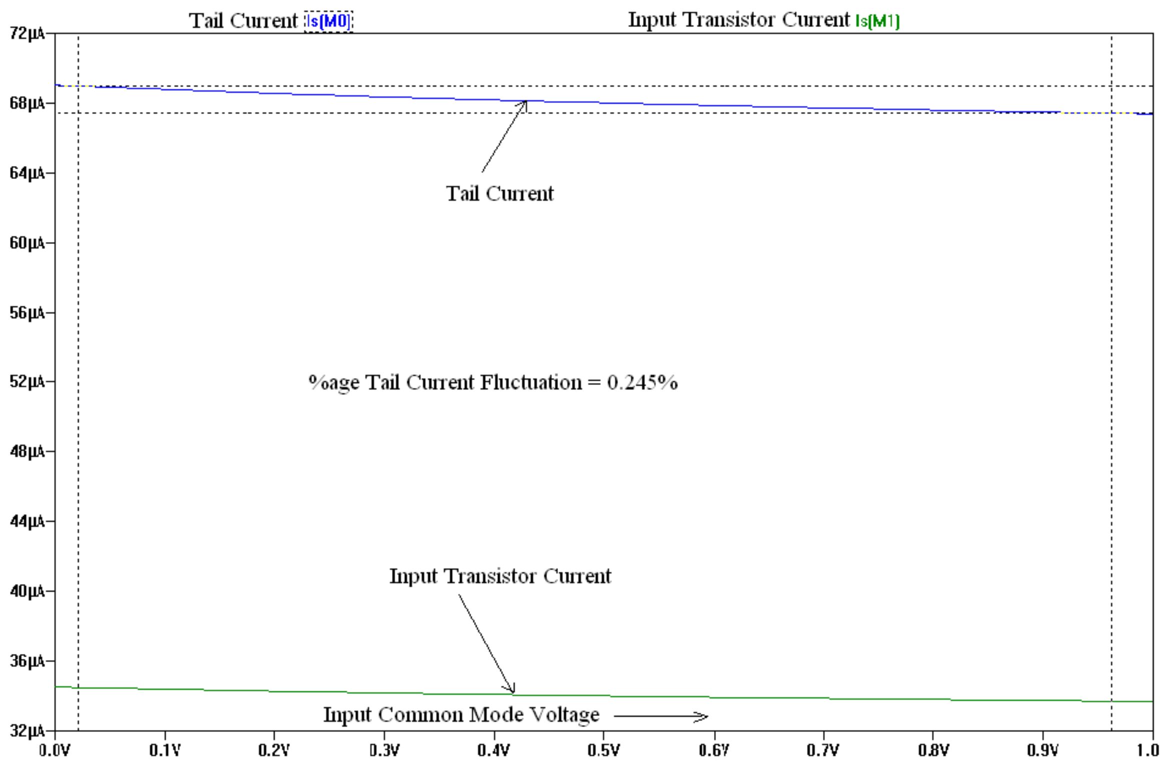


Fig.4.6 Input common mode range of rail to rail Op-amp

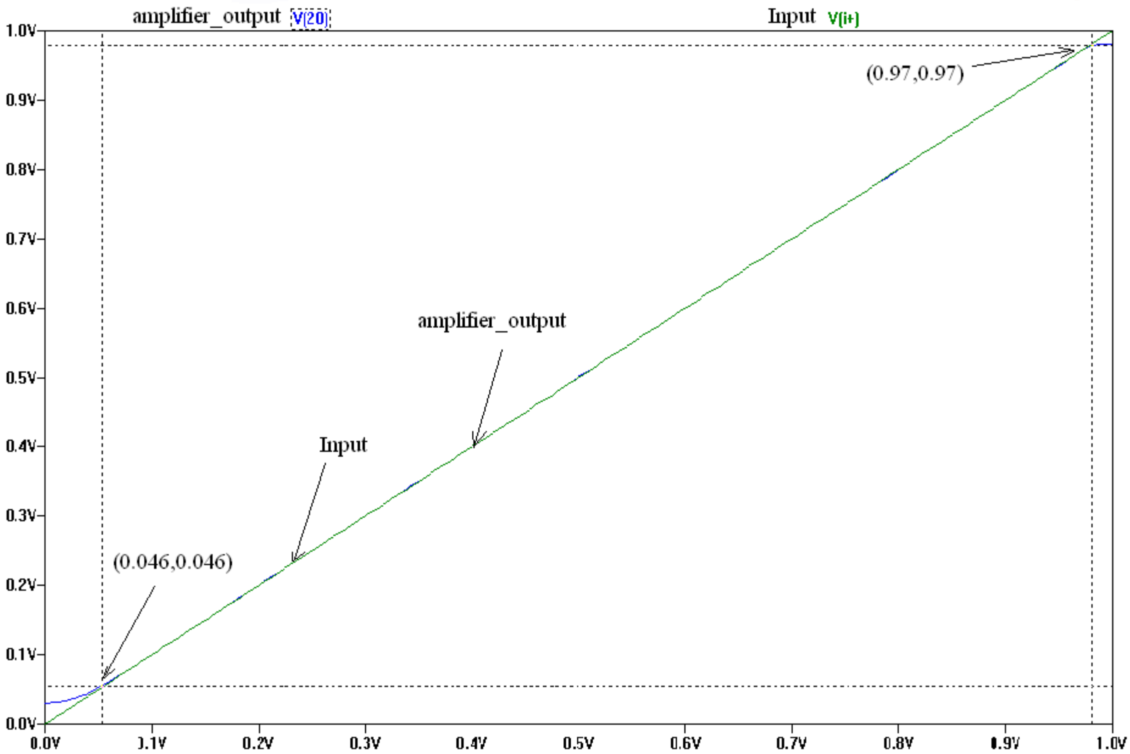


Fig.4.7 Transient response of a rail to rail Op-amp connected in unity gain configuration

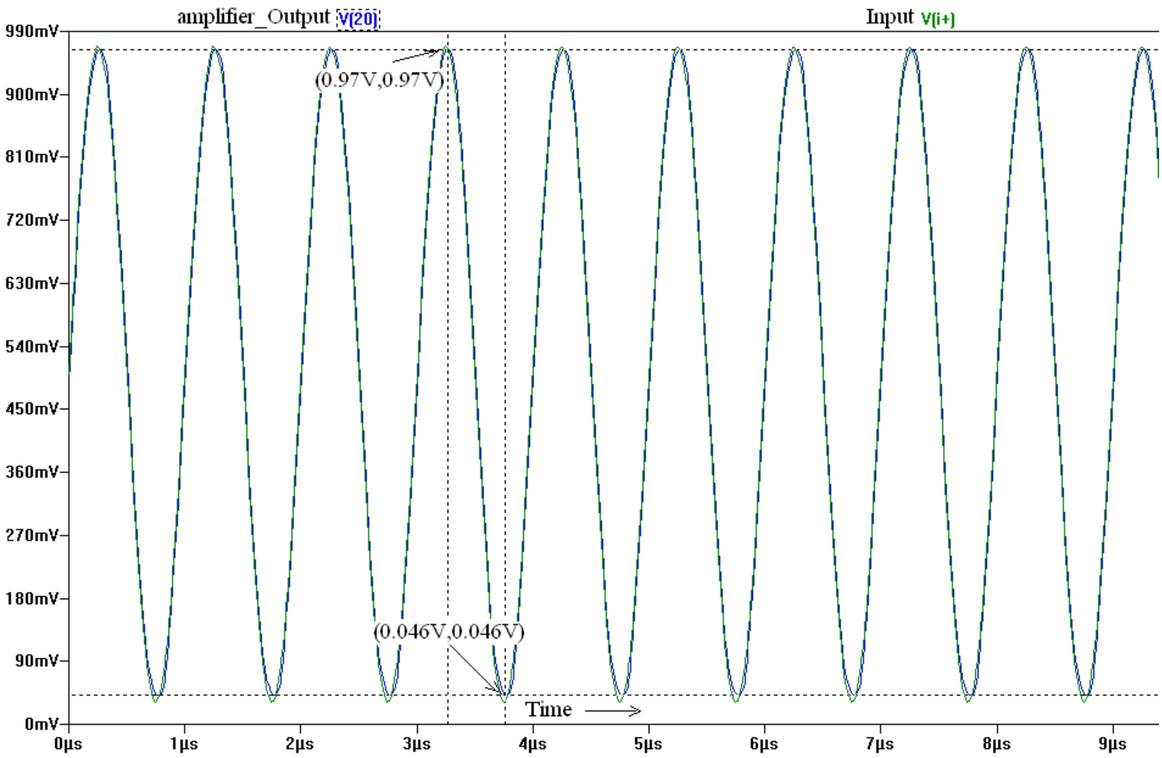


Fig.4.8 Transient response of a rail to rail Op-amp connected in unity gain configuration for sinusoidal signal of 0.894 Vpp

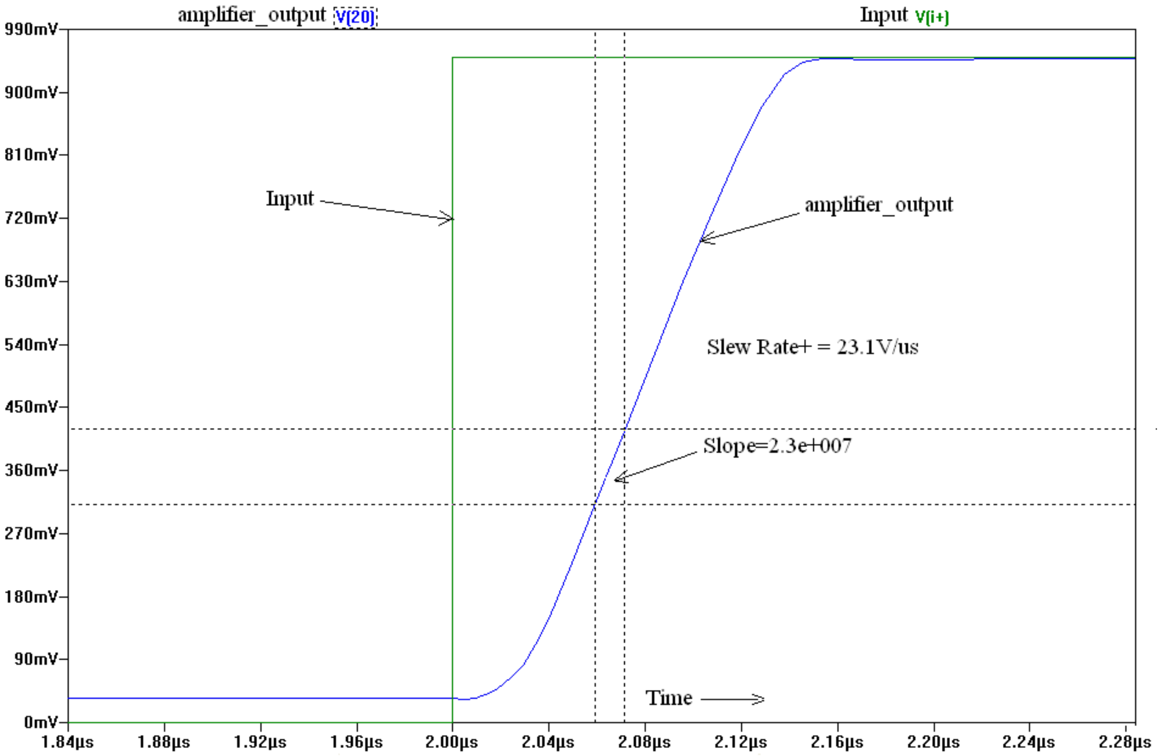


Fig.4.9 Positive Slew rate of rail to rail Op-amp

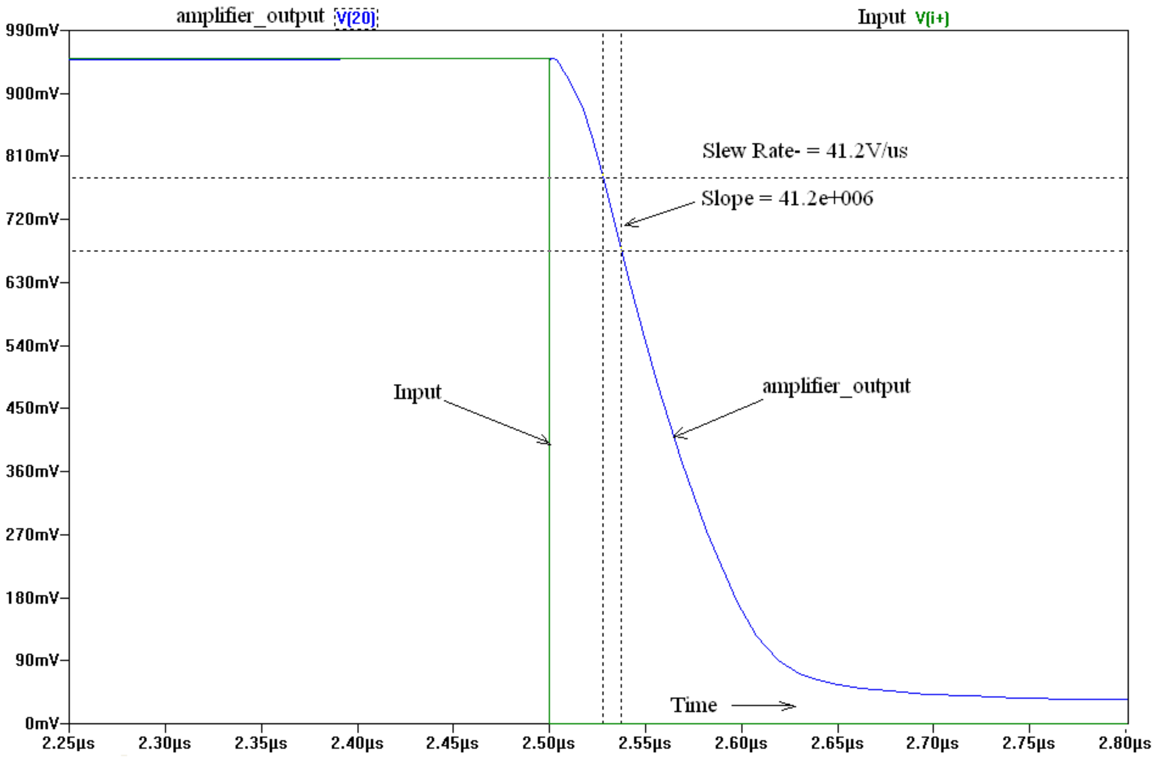


Fig.4.10 Negative Slew rate of rail to rail Op-amp

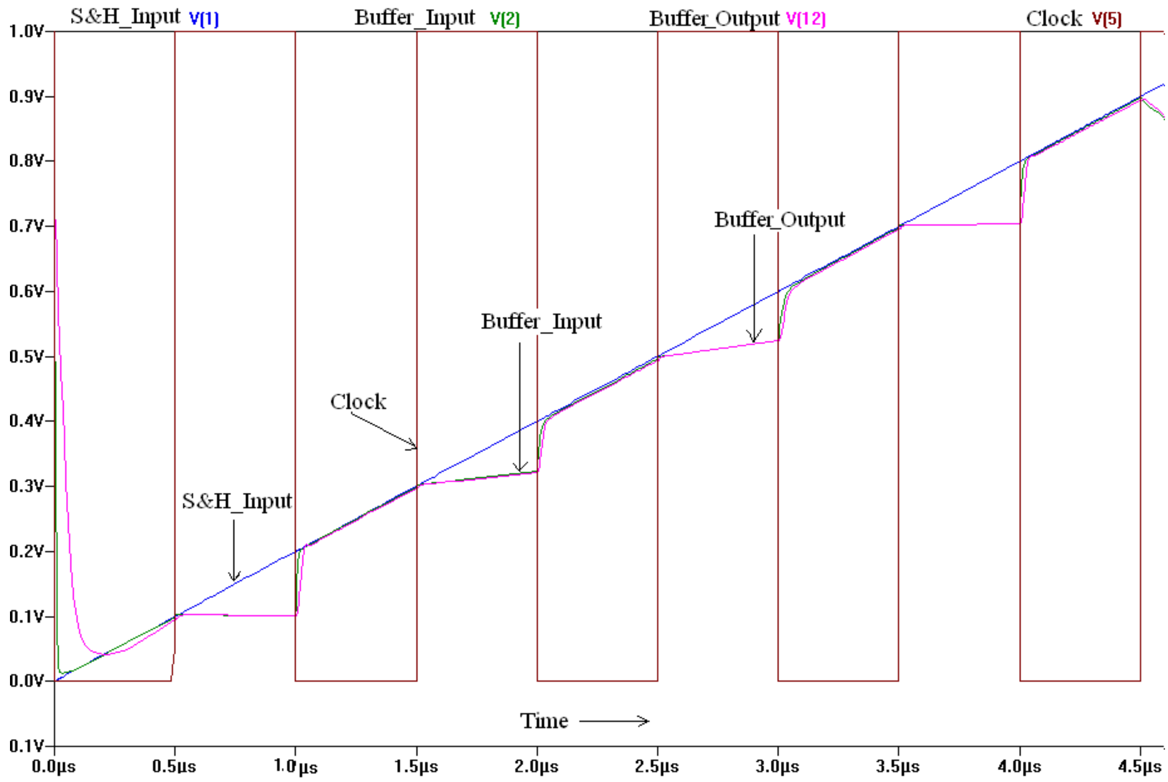


Fig.4.11 Sample & Hold circuit response to a ramp input signal.

4.4 Discussion of Results:

Fig.4.1 shows the dc characteristics of the Input CM adapter circuit. It shows that the output of CM adapter circuit is fixed to a reference voltage for input that varies from rail to rail. A little deviation of the output from a fixed reference voltage occurs due to the channel length modulation but that doesn't create problem as long as this variation is under the input common mode range of the p channel input differential pair.

Fig.4.2 shows that the input and output DM of CM Adapter circuit are approximately equal. So, this implies that the negative feedback in the CM adapter circuit affects only the common mode part of the input signal and differential mode component remains unaffected.

Fig.4.3 shows that the negative feedback loop employed in the CM Adapter circuit is stable. The phase margin confirms its stability.

Fig.4.4 shows the frequency response curve of the complete rail to rail amplifier. Gain of 75.3dB with a unity gain bandwidth of 30.26MHz is achieved. The Phase Margin is 58.3° for a load capacitor of 3.5pF and a compensation capacitor of 1.5pF.

Fig.4.5 gives the input common mode range of the amplifier using p channel differential pair before using the Input CM adapter circuit.

Fig.4.6 gives the improved common mode range after using the Input CM Adapter circuit. The input common mode range varies from rail to rail. The tail current fluctuation as low as ±0.245% is achieved due to accurate action of negative feedback employed in Input CM adapter circuit.

Fig.4.7 & 4.8 shows the transient response of the complete rail to rail Operational amplifier connected in unity gain configuration. A sinusoidal response of the unity gain buffer is shown in Fig.4.8 for 0.894 Vpp.

Fig.4.9 & 4.10 gives the positive and negative slew rates of the complete rail to rail Operational amplifier. The positive and negative slew rates obtained are 23.1 V/µs and 41.2 V/µs respectively for a tail current of 68.5µA.

Fig.4.11 shows the sample and hold output with respect to the ramp input applied. The clock frequency of 1MHz with a sampling capacitor of 10pF is achieved.

Chapter 5
Conclusion and Future Work

5.1 Conclusion:

A low voltage rail to rail Operational amplifier using the single differential pair employing the dynamic level shifting technique has been designed in 0.18µm technology. The amplifier resolves the problems which occur at low voltages by providing rail to rail swing at the input. This amplifier has been used successfully as a unity gain buffer in the design of sample and hold circuit for use in pipeline ADC having 10 bit resolution and a speed of 1 MSPS speed.

A Novelty has been introduced in the Input CM adapter circuit to work for input common mode voltage less than the reference voltage and a low value of gm fluctuation ±0.245% is achieved using the dynamic level shifting technique which is a low value among the standard CMOS implementation of Operational amplifier using single n or p channel differential pair.

The amplifier gives a gain of 75.3dB with an output voltage swing of 0.894 volts and a CMRR of 108dB.

Future work lies in designing the amplifier to give rail to rail output swing. Also, the concept of dynamic level shifting can be utilized fully by replacing passive level shift resistors with an active counterpart in the Input CM Adapter circuit for tackling the problems occurred due to the passive resistors.

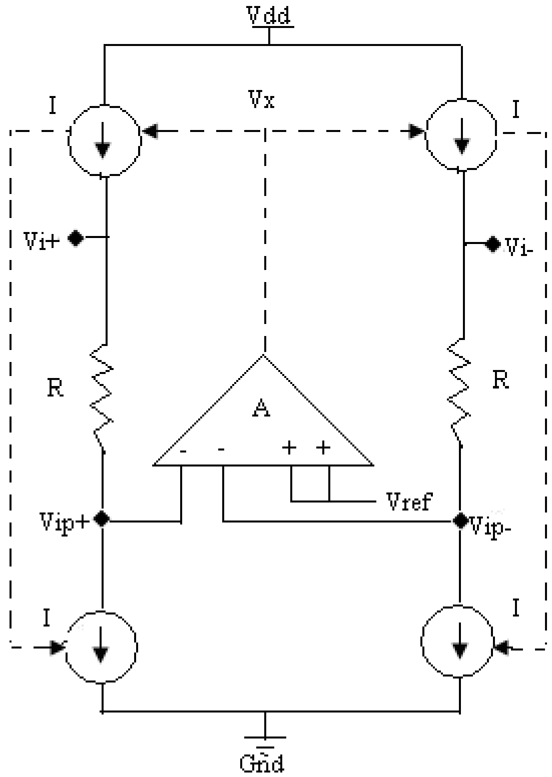
The channel length modulation effect become severe as the technology downscales. The pseudo-differential structure which is used to implement the input CM Adapter circuit can be modified for tackling the problems due to channel length modulation.

The complete Operational amplifier can be designed to achieve high speed by employing extra bias circuitry for high slew rate.

Appendices

Appendix I

Fig.3.1.1 below shows Input CM adapter circuit consisting of feedback amplifier having open loop gain A whose output control the current sources responsible for fixing the output node to a known reference voltage.



We can write,

$$V_{ip+} = V_{i+} - I*R \quad \text{-------------------(1)}$$

$$V_{ip-} = V_{i-} - I*R \quad \text{-------------------(2)}$$

<u>For Vip,cm</u>:

From (1) and (2)

$$V_{ip,cm} = V_{i,cm} - I*R \quad \text{-------------------(3)}$$

$$I = -Gm*Vx$$

Output Vx of error amplifier in its linear region will be equal to

$$Vx = A[2*Vref - (V_{ip+} + V_{ip-})]$$

$$= 2*A*(Vref - V_{ip,cm}) \quad \text{-------------------(4)}$$

Therefore, $I = - Gm^* 2*A*(Vref – Vip,cm)$ --------------------(5)

From (3) & (6),

$$Vip,cm = Vi,cm + Gm*2*A*R*(Vref – Vip,cm)$$

$$Vip,cm(1+ Gm*2*A*R) = Vi,cm + Gm*2*A*R*Vref$$

$$Vip,cm = Vref + \frac{Vi,cm}{Gm*2*A*R} \qquad \text{--------------------(6)}$$

<u>For Vip,dm</u> :

$$Vip_+ - Vip_- = (Vi_+ - I*R) - (Vi_- - I*R)$$

$$Vip,dm = Vi,dm \qquad \text{--------------------(7)}$$

Where,

Vip,cm &Vip,dm → CM & DM component of the output signals Vip_+ and Vip_- respectively.

Vi,cm &Vi,dm → CM & DM component of the input signals Vi_+ and Vi_- respectively.

A → Finite dc gain of the feedback (error) amplifier.

Vref → Fixed reference voltage.

Gm → Transconductance of voltage controlled current source I.

R → Resistor.

Apendix II

Spice File for Rail to Rail Operational amplifier designed at 1V

v(20) is the output node

v(32) is non inverting input of p- channel single differential pair

v(33) is inverting input of p- channel single differential pair

***v(i+), v(i-)non inverting and inverting input terminals of complete rail to rail operational amplifier

***

*.subckt folded_opamp i+ i- 20

****

*Supply Section

****

VDD 100 0 1

vref1 ref1 0 0.35

vref2 ref2 0 0.2

****

*Widths and Lengths

****

.params w_0=47.4u l_0=0.90u

.params w_1=23.7u l_1=0.90u

.params w_2=23.7u l_2=0.90u

.params w_3=23.465u l_3=0.90u

.params w_4=21.13u l_4=0.90u

.params w_5=21.13u l_5=0.90u

.params w_6=23.465u l_6=0.90u

.params w_7=140.7u l_7=0.90u

.params w_8=42.66u l_8=0.90u

.params w_9=42.66u l_9=0.90u

.params w_10=140.7u l_10=0.90u

.params w_11=13.76u l_11=0.18u

.params w_12=60.256u l_12=0.18u

***Input CM Adapter circuit instantiation

x1 i+ i- 32 33 cm_adapter

***Tail current source

M0 11 ref1 100 100 cmosp w={w_0} l={l_0} AD={1.25*w_0*l_0} AS={1.25*w_0*l_0} PD={5*l_0+w_0} PS={5*l_0+w_0}

**Input differential pair of PMOS Input OpAMP

M1 8 32 11 100 cmosp w={w_1} l={l_1} AD={1.25*w_1*l_1} AS={1.25*w_1*l_1} PD={5*l_1+w_1} PS={5*l_1+w_1}

M2 10 33 11 100 cmosp w={w_2} l={l_2} AD={1.25*w_2*l_2} AS={1.25*w_2*l_2} PD={5*l_2+w_2} PS={5*l_2+w_2}

*** Cascode stage

M3 9 100 10 0 cmosn w={w_3} l={l_3} AD={1.25*w_3*l_3} AS={1.25*w_3*l_3} PD={5*l_3+w_3} PS={5*w_3+l_3}

M4 10 9 0 0 cmosn w={w_4} l={l_4} AD={1.25*w_4*l_4} AS={1.25*w_4*l_4} PD={5*l_4+w_4} PS={5*l_4+w_4}

M5 8 9 0 0 cmosn w={w_5} l={l_5} AD={1.25*w_5*l_5} AS={1.25*w_5*l_5} PD={5*l_5+w_5} PS={5*l_5+w_5}

M6 7 100 8 0 cmosn w={w_6} l={l_6} AD={1.25*w_6*l_6} AS={1.25*w_6*l_6} PD={5*l_6+w_6} PS={5*l_6+w_6}

M7 7 ref2 4 100 cmosp w={w_7} l={l_7} AD={1.25*w_7*l_7} AS={1.25*w_7*l_7} PD={5*l_7+w_7} PS={5*l_7+w_7}

M8 4 ref1 100 100 cmosp w={w_8} l={l_8} AD={1.25*w_8*l_8} AS={1.25*w_8*l_8} PD={5*l_8+w_8} PS={5*l_8+w_8}

M9 5 ref1 100 100 cmosp w={w_9} l={l_9} AD={1.25*w_9*l_9} AS={1.25*w_9*l_9} PD={5*l_9+w_9} PS={5*l_9+w_9}

M10 9 ref2 5 100 cmosp w={w_10} l={l_10} AD={1.25*w_10*l_10} AS={1.25*w_10*l_10} PD={5*l_10+w_10} PS={5*l_10+w_10}

*** Output Stage

M12 20 ref1 100 100 cmosp w={w_12} l={l_12} AD={1.25*w_12*l_12} AS={1.25*w_12*l_12} PD={5*l_12+w_12} PS={5*l_12+w_12}

M11 20 7 0 0 cmosn w={w_11} l={l_11} AD={1.25*w_11*l_11} AS={1.25*w_11*l_11} PD={5*l_11+w_11} PS={5*l_11+w_11}

```
****Compensation capacitor and miller resistors
Rm 7 201 3k
cc 201 20 1.5p
cl 20 0 3.5p
******************************************
*dc analysis without CM Adapter Circuit
******************************************
*Vi+ 32 0 200.04m
*vi- 33 32
* 0 200.04m
*.dc Vi+ 0 1 0.0001
*.op
******************************************
*ac analysis without CM Adapter Circuit
*****************************************
*Vi+ 32 0 dc={x} ac = 1
*vi- 33 0 dc={x} ac =1
*.param x=0.2
*.step param x list 0 0.1 0.2 0.3 0.35 0.38 0.4 0.5 0.6 0.7 0.8 0.9 1
*.ac dec 10 1 1G 10
******************************************
*Transient analysis without CM Adapter Circuit
*******************************************
*Vi+ 32 0 0.2 ac= 0.5 sin(0.2 20u 0.5Mega)
*Vi- 33 0 0.2 ac=-0.5 sin(0.2 -20u 0.5Mega)
*.trans 0 10u 0.00001u
*.tf V(7) Vi+
*.op
******************************************
**unity gain mode without CM Adapter Circuit
******************************************
*Vi+ 32 0 pulse(0 1 0.001n 0.001n 0.001n 0.5u 1u 100)
```

```
**ac=1v sin(.4 .4 20k)
*vx 33 20 0
*.trans 0 1m 0.1m
*.ac dec 10 1 1G
*.dc Vi+ 0 1 0.0001
********************************************
*dc analysis using CM Adapter
********************************************
*Vi+ i+ 0 200.04m
*vi- i- 20
*.op
*.dc Vi+ 0 1 0.0001
********************************************
*Transient analysis using CM Adapter Circuit
*********************************************
*Vi+ i+ 0 pulse(0 0.95 0.001n 0.001n 0.001n 0.5u 1u 100)
*Vi+ i+ 0 0.2 ac= 1 sin(0.5 0.43 1Meg)
*Vi- i- 20
*.trans 0 15u 0.00001u
**********************
*AC analysis using CM Adapter
***********************
*Vi+ i+ 0 dc={x} ac 1
*vi- i- 0 dc={x} ac 1
*.param x=0.2
*.step param x list 0 0.1 0.2 0.3 0.35 0.38 0.4 0.5 0.6 0.7 0.8 0.9 1
*.ac dec 10 1 1G
*.ends
.subckt cm_adapter 8 9 3 4
****Widths and Lengths section
.params w_c1=1.20u l_c1=0.90u
.params w_c2=1.20u l_c2=0.90u
```

```
.params w_c3=24.48u l_c3=0.90u
.params w_c4=24.48u l_c4=0.90u
*********
.params w_1=0.868u l_1=1.26u
.params w_2=0.868u l_2=1.26u
.params w_3=0.868u l_3=1.26u
.params w_4=0.868u l_4=1.26u
.params w_5=24.58u l_5=0.90u
**********
.params w_6=24.58u l_6=0.90u
.params w_7=24.58u  l_7=0.90u
.params w_8=12.13u l_8=1.98u
.params w_9=84.96u l_9=0.90u
*********
.params w_10=84.96u l_10=0.90u
.params w_11=84.96u l_11=0.90u
.params w_12=93.8u  l_12=2.88u
.params w_13=93.8u  l_13=2.88u
*********
.params w_14=7.99u l_14=0.90u
.params w_15=7.99u l_15=0.90u

****VREF DIFFERENTIAL PAIR

M1 2 ref0 100 100 cmosp w={w_1} l={l_1} AD={1.25*w_1*l_1} AS={1.25*w_1*l_1} PD={5*l_1+w_1} PS={5*l_1+w_1}
M2 2 ref0 100 100 cmosp w={w_2} l={l_2} AD={1.25*w_2*l_2} AS={1.25*w_2*l_2} PD={5*l_2+w_2} PS={5*l_2+w_2}

****Input differential pair of CM ADAPTER

M3 5 3 100 100 cmosp w={w_3} l={l_3} AD={1.25*w_3*l_3} AS={1.25*w_3*l_3} PD={5*l_3+w_3} PS={5*l_3+w_3}
```

```
M4 5 4 100 100 cmosp w={w_4} l={l_4} AD={1.25*w_4*l_4} AS={1.25*w_4*l_4}
PD={5*l_4+w_4} PS={5*l_4+w_4}
***Novelty
Mtry 88 5 0 0 cmosn w={w_c1} l={l_c1} AD={1.25*w_c1*l_c1}
AS={1.25*w_c1*l_c1} PD={5*l_c1+w_c1} PS={5*l_c1+w_c1}
Mtry1 99 5 0 0 cmosn w={w_c2} l={l_c2} AD={1.25*w_c2*l_c2}
AS={1.25*w_c2*l_c2} PD={5*l_c2+w_c2} PS={5*l_c2+w_c2}
MC3 3 7 100 100 cmosp w={w_c3} l={l_c3} AD={1.25*w_c3*l_c3}
AS={1.25*w_c3*l_c3} PD={5*l_c3+w_c3} PS={5*l_c3+w_c3}
MC4 4 7 100 100 cmosp w={w_c4} l={l_c4} AD={1.25*w_c4*l_c4}
AS={1.25*w_c4*l_c4} PD={5*l_c4+w_c4} PS={5*l_c4+w_c4}
*****Current Sources
M5 3 7 0 0 cmosn w={w_5} l={l_5} AD={1.25*w_5*l_5} AS={1.25*w_5*l_5}
PD={5*l_5+w_5} PS={5*l_5+w_5}
M6 4 7 0 0 cmosn w={w_6} l={l_6} AD={1.25*w_6*l_6} AS={1.25*w_6*l_6}
PD={5*l_6+w_6} PS={5*l_6+w_6}
M7 10 7 0 0 cmosn w={w_7} l={l_7} AD={1.25*w_7*l_7} AS={1.25*w_7*l_7}
PD={5*l_7+w_7} PS={5*l_7+w_7}
M8 7 100 10 0 cmosn w={w_8} l={l_8} AD={1.25*w_8*l_8} AS={1.25*w_8*l_8}
PD={5*l_8+w_8} PS={5*l_8+w_8}
*v7 7 10 0
*****
M9 7 5 100 100 cmosp w={w_9} l={l_9} AD={1.25*w_9*l_9} AS={1.25*w_9*l_9}
PD={5*l_9+w_9} PS={5*l_9+w_9}
M10 8 5 100 100 cmosp w={w_10} l={l_10} AD={1.25*w_10*l_10}
AS={1.25*w_10*l_10} PD={5*l_10+w_10} PS={5*l_10+w_10}
M11 9 5 100 100 cmosp w={w_11} l={l_11} AD={1.25*w_11*l_11}
AS={1.25*w_11*l_11} PD={5*l_11+w_11} PS={5*l_11+w_11}
***
```

```
M12 2 2 100 100 cmosp w={w_12} l={l_12} AD={1.25*w_12*l_12}
AS={1.25*w_12*l_12} PD={5*l_12+w_12} PS={5*l_12+w_12}
M13 5 2 100 100 cmosp w={w_13} l={l_13} AD={1.25*w_13*l_13}
AS={1.25*w_13*l_13} PD={5*l_13+w_13} PS={5*l_13+w_13}

*** Total Current
M14 2 ref1 0 0 cmosn w={w_14} l={l_14} AD={1.25*w_14*l_14}
AS={1.25*w_14*l_14} PD={5*l_14+w_14} PS={5*l_14+w_14}
M15 5 ref1 0 0 cmosn w={w_15} l={l_15} AD={1.25*w_15*l_15}
AS={1.25*w_15*l_15} PD={5*l_15+w_15} PS={5*l_15+w_15}
*v_dull 5 6 0
R3 8 88 10k
R4 9 99 10k
R1 88 3 5k
R2 99 4 5k
CL 5 0 0.5p
vref ref0 0 0.2
*vref2 ref2 0 0
vtotal ref1 0 0.52
VDD 100 0 1
*vi+ 8 0 0.98
* dc={x} ac=1 sin(0.4 0.3m 20k)
*vi- 9 8
*dc={x} ac=1 sin(0.4 -0.3m 20k)
*0 0.5 ac -0.5
*.param x=0
*.trans 0 10m 0.001m
*.dc vi+ 0 1 0.01
;.op
*.ac dec 10 1 1G
.ends
```

0.18μm Spice Model Parameters:

```
.MODEL CMOSN NMOS (                LEVEL   = 8
+VERSION = 3.1         TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7        NCH     = 2.3549E17   VTH0    = 0.3615019
+K1      = 0.5839709   K2      = 2.711646E-3 K3      = 1E-3
+K3B     = 3.3983311   W0      = 1E-7        NLX     = 1.740455E-7
+DVT0W   = 0           DVT1W   = 0           DVT2W   = 0
+DVT0    = 1.6795734   DVT1    = 0.5014497   DVT2  =-5.405309E-3
+U0      = 293.6913905 UA      = -1.172299E-9 UB     = 2.233278E-18
+UC      = 3.726817E-11 VSAT   = 1.044979E5  A0      = 1.9381397
+AGS     = 0.4141981   B0      = -1.06866E-8 B1      = -1E-7
+KETA    = -5.193294E-3 A1     = 3.652366E-4 A2      = 0.8786185
+RDSW    = 150         PRWG    = 0.5         PRWB    = -0.110601
+WR      = 1           WINT    = 0           LINT    = 9.896345E-9
+XL      = -2E-8       XW      = -1E-8       DWG     = -1.819021E-9
+DWB     = 1.332852E-8 VOFF    = -0.0892938  NFACTOR = 2.5
+CIT     = 0           CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB   = 0           ETA0    = 2.591694E-3 ETAB    = 1.375566E-4
+DSUB    = 0.012994    PCLM    = 0.7743192   PDIBLC1 = 0.1028762
+PDIBLC2 = 2.336026E-3 PDIBLCB = -0.1        DROUT   = 0.736696
+PSCBE1  = 8E10        PSCBE2  = 1.954508E-7 PVAG    = 5.582843E-3
+DELTA   = 0.01        RSH     = 6.7         MOBMOD  = 1
+PRT     = 0           UTE     = -1.5        KT1     = -0.11
+KT1L    = 0           KT2     = 0.022       UA1     = 4.31E-9
+UB1     = -7.61E-18   UC1     = -5.6E-11    AT      = 3.3E4
+WL      = 0           WLN     = 1           WW      = 0
+WWN     = 1           WWL     = 0           LL      = 0
+LLN     = 1           LW      = 0           LWN     = 1
+LWL     = 0           CAPMOD  = 2           XPART   = 0.5
+CGDO    = 7.59E-10    CGSO    = 7.59E-10    CGBO    = 1E-12
+CJ      = 9.633805E-4 PB      = 0.7217456   MJ      = 0.3598664
+CJSW    = 2.344029E-10 PBSW   = 0.7815199   MJSW    = 0.1
+CJSWG   = 3.3E-10     PBSWG   = 0.7815199   MJSWG   = 0.1
```

```
+CF      = 0              PVTH0   = -1.6855558E-3  PRDSW   = -2.9244849
+PK2     = 5.819772E-4    WKETA   = -1.343618E-3   LKETA   = -8.510896E-3
+PU0     = 2.9548717      PUA     = -6.80592E-12   PUB     = 0
+PVSAT   = 1.206584E3     PETA0   = 1.0E-4         PKETA   = 4.054473E-3    )
*
.MODEL CMOSP PMOS (                                LEVEL   = 8
+VERSION = 3.1            TNOM    = 27             TOX     = 4.1E-9
+XJ      = 1E-7           NCH     = 4.1589E17      VTH0    = -0.3931011
+K1      = 0.568234       K2      = 0.0266293      K3      = 0
+K3B     = 10.2425067     W0      = 1E-6           NLX     = 9.914676E-8
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.             DVT1    = 0.3116518      DVT2    = 0.1
+U0      = 116.2567314    UA      = 1.547573E-9    UB      = 1E-21
+UC      = -1E-10         VSAT    = 1.523056E5     A0      = 1.6918373
+AGS     = 0.4085242      B0      = 1.01169E-6     B1      = 3.39099E-6
+KETA    = 0.0195051      A1      = 0.8            A2      = 0.3921219
+RDSW    = 383.5720896    PRWG    = 0.5            PRWB    = 0.1197139
+WR      = 1              WINT    = 0              LINT    = 2.113742E-8
+XL      = -2E-8          XW      = -1E-8          DWG     = -3.132884E-8
+DWB     = 8.668675E-9    VOFF    = -0.1004133     NFACTOR = 2
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 0.0324741E-3   ETAB    = -0.049336
+DSUB    = 0.6814806      PCLM    = 1.1567401      PDIBLC1 = 4.261071E-4
+PDIBLC2 = 0.0210377      PDIBLCB = -1E-3          DROUT   = 2.603105E-4
+PSCBE1  = 9.161756E9     PSCBE2  = 2.64613E-9     PVAG    = 3.3911231
+DELTA   = 0.01           RSH     = 7.5            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 6.61E-10       CGSO    = 6.61E-10       CGBO    = 1E-12
```

```
+CJ      = 1.207043E-3    PB       = 0.854724       MJ       = 0.409169
+CJSW    = 1.902789E-10   PBSW     = 0.6154466      MJSW     = 0.2504159
+CJSWG   = 4.22E-10       PBSWG    = 0.6154466      MJSWG    = 0.2504159
+CF      = 0              PVTH0    = 2.14283E-3     PRDSW    = -2.3142803
+PK2     = 1.460103E-3    WKETA    = 0.0158438      LKETA    = -4.304888E-3
+PU0     = -1.9357794     PUA      = -6.33937E-11   PUB      = 1E-21
+PVSAT   = -50            PETA0    = 1E-4           PKETA    = -7.652238E-4    )
*
```

Appendix III

MOS Switch:

Using an nMOS Switch in the sample and hold circuit has mainly two problems:

Input dependent finite on Resistance

The on resistance Ron of MOS switch operating in triode region is given by:

$$R_{on} = \left(\frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right) \left(V_{gs} - V_t\right)} \right)$$

Since Vgs is equal to Vdd – Vin, Ron depends upon Vin which causes harmonic distortion. Also, since Vdd is small, Vgs is small and hence in order to make Ron small for wideband track signal, the W/L has to increase which in turn causes large charge injection.

Input dependent charge Injection:

When the MOS switch turns off, then the charge stored in the channel has to go somewhere. This channel charge is distributed over the sampling capacitor whose magnitude is given by:

$$Q_{ch} \approx WLC_{ox}(V_{gs} - V_t)$$

Now since Vgs is equal to Vdd – Vin in the sample and hold circuit, Qch depends upon Vin which causes pedestal errors.

Non-Idealities in Sample and Hold Circuit:

1. Finite acquisition time.
2. KT/C Noise.
3. Aperture uncertainty.
4. Signal dependent sampling instant.
5. Hold mode feed through and droop.
6. Track mode uncertainty.
7. Pedestal error, Charge Injection.

Compensation for Non-Idealities:

1. CMOS Switch, Clock Boosting.
2. Dummy Switch.
3. Full Differential bottom Plate Sampling.

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