Design of Voltage Reference Circuits

by

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A Thesis Submitted in Partial Fulfilment of the Requirements for the Degree of

Master of Technology

in

Information and Communication Technology

to

Dhirubhai Ambani Institute of Information and Communication Technology

May, 2008

Declaration

This is to certify that

(i) The thesis comprises my original work towards the degree of Master of Technology in Information and Communication Technology at DA-IICT and has not been submitted elsewhere for a degree,

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This is to certify that the thesis work entitled "**Design of Voltage reference circuits**" has been carried out by Bhavi Panchal (200611020) for the degree of Master of Technology in Information and Communication Technology at this Institute under my/our supervision.

Dr. Chetan Parikh

Abstract

Shrinking device dimensions in advancing CMOS technologies require lower supply voltages to ensure device reliability. As a result, analog circuit designers are faced with many challenges in finding new ways to build analog circuits that can operate at lower supply voltages while maintaining performance. Bandgap references are subject to these head-room problems especially when the required supply voltage approaches the bandgap voltage of silicon. However, the bandgap reference working with a low supply voltage often has a higher temperature coefficient than that of a traditional bandgap reference. This has resulted in the development of new temperature-compensated techniques.

Piecewise linear curvature correction method is simple yet robust technique which was previously available in bipolar technology. This research work describes a Novel CMOS bandgap reference which uses piecewise-linear curvature compensation scheme for second order correction. In standard 0.18μm CMOS process, the reference, with 1.8 V supply produces an output of about 928 mV, which varies by 160 μV from -25 °C to 150°C. It dissipates 150 μW and has a DC PSRR of -46 dB.

Acknowledgements

This thesis owes its existence to the help, support, and inspiration of many people. It is a pleasure to convey my gratitude to them all in my humble acknowledgment.

In the first place I would like to record my gratitude to Dr. Chetan Parikh for his supervision, advice, and guidance as well as giving me his extraordinary experiences through out the work. He not only introduced me to wonderful world of analog and mixed-signal circuits design but also gave me an opportunity to work in the field of VLSI. With every weekly discussion, I used to find myself more focused, enriched and motivated; it used to change my outlook in analyzing complex circuits tremendously. He is a constant source of inspiration and has enriched my growth as a student, a researcher. I am indebted to him more than he knows.

I am also very thankful to Kallol Chatterjee from STMicroelectronics for his kind guidance and encouragement. His suggestions and critical comments has been a great help in improving quality of this work.

I am deeply indebted to my committee members Prof. Dipankar Nagchoudhuri and Sushanta Kumar Mandal for their time and effort in reviewing this work.

I would also acknowledge Akhil Rathore, Garima Bajaj, Vivek Verma and Prashant Bambhaniya for their advice and their willingness to share their bright thoughts with me, which were very fruitful for shaping up my ideas and research.

Finally, I would like to express my deepest gratitude for the constant support and love that I received from my parents and my brother during the past years.

Above all, this thesis is dedicated to my parents. Their love and support in all that I have done till now are the keys of all my achievements.

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List of Principal Symbols and Acronyms

ADC	Analog to digital converter
BGR	Bandgap voltage reference
BSIM	Berkeley Short-Channel IGFET Model for MOS
BJT	Bipolar junction transistor
CTAT	Complementary to absolute temperature
DAC	Digital to analog converter
DC	Direct current
DTMOS	Dynamic threshold metal oxide semiconductor
MNC	Matched nonlinear compensation
OTA	Operational transconductance amplifier
PSRR	Power supply rejection ration
PTAT	Proportional to absolute temperature
TC	Temperature coefficient
V_T	Thermal voltage
δ	Temperature dependence of collector current of BJT
η	Temperature independent and process dependent constant
k	Boltzmann's constant
q	Electron charge
A	Gain from input node to output node
A_p	Gain from power node to output node
R	Resistance

I	Current
GBW	Gain bandwidth product

1. INTRODUCTION

1.1.General

Voltage reference is used as basic building block in many analog & mixed signal circuits such as On-Chip voltage references in ADC and DAC, Voltage regulators, Measurement System, DRAM, Flash memories etc.

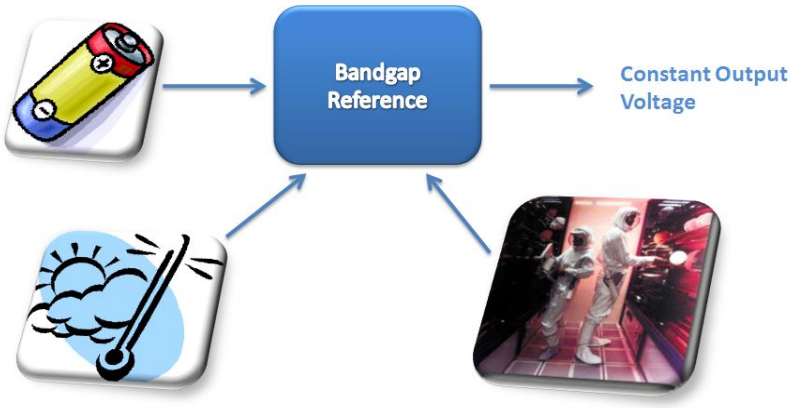


Figure 1 Ideal Reference

Ideal Reference as shown in figure 1 generates output independent of supply voltage, temperature and process. As most of the process parameters are temperature dependent, reference which gives temperature independent output is also said to be process independent.

Common realization of voltage reference is using Zener diode, which is not suitable for low voltage and high precision application. Such reference is called zero-order reference because there is no effort on the part of the designer to improve initial accuracy [1]. So an alternative concept of Bandgap voltage reference was proposed in 1964 [2] and first Bandgap voltage reference circuit was proposed in 1971 [3] using BJT, though circuit proposed by K. Kujik in 1973 [4] is most widely used structure which is often called conventional Bandgap voltage reference (BGR).

Principle of operation of Bandgap voltage reference can be explained as follows. If two quantities with opposite temperature coefficient are added with proper weighting, the resultant quantity theoretically exhibits zero temperature coefficients [5]. Conventionally quantity with negative temperature coefficient is forward baised junction voltage and with positive temperature coefficient is thermal voltage.

1.2.Research Objectives and Scope

Primarily, the objectives of this research work are the following

- To design the Bandgap voltage reference (BGR) to meet the specification provided by STMicroelectronics.
- To design Piecewise Linear Curvature corrected CMOS BGR

Precision BGR are always in great demand in many applications because typical first-order bandgap references are no longer adequate for many high-performance systems. As a result, many higher-order temperature compensation techniques to improve the temperature coefficient (TC) of BGR has been Proposed [6]-[12]. Reference [12] uses simple yet robust technique of piecewise-linear correction, but it is implemented in bipolar technology.

For the fulfillment of second objective, in this research work, an all CMOS bandgap voltage reference using a piecewise-linear curvature-correction method is introduced. For the fulfillment of first objective, 2.7 V first order BGR in 0.18μm technology is designed.

1.3.Thesis Organization

Chapter 2 introduces the topic of bandgap voltage reference (BGR). The general topics discussed include performance metrics of typical BGR, Temperature dependence of the diode voltage and output stage of the reference.

Chapter 3 summarizes the various techniques to improve the performance of first order voltage reference. End of the chapter 3 describes the alternative solution to BGR; A CMOS voltage reference based on MOS characteristics.

Chapter 4 deals with the design of improved PSRR BGR; it also contains the PSRR analysis of voltage mode BGR, performance summary and simulated results for designed circuit. **Chapter 5** describes the proposed piecewise linear curvature corrected BGR. It concludes the chapter by providing performance summary and simulated results.

Chapter 6 concludes this dissertation with the mentioning some of the achievements, contribution of this research and the scope of future work.

2. BACKGROUND

2.1.Conventional BGR Circuit

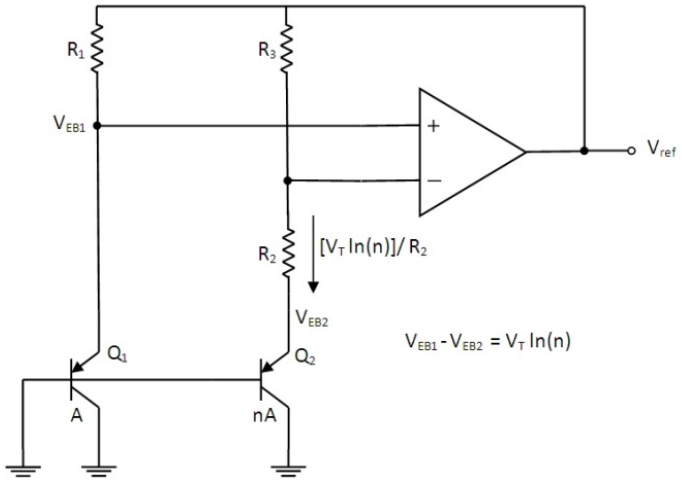


Figure 2 Conventional BGR circuit

The base-emitter voltage (V_{BE}) of BJT or, more generally, the forward voltage of a pn-junction exhibits a negative Temperature Coefficient (TC) typically -2 mV/°C. It is shown in [2] that if two BJT operate at unequal current densities, then the difference between their V_{BE} is directly proportional to the absolute temperature. So the basic idea is to add a PTAT (Proportional to absolute temperature) voltage to a negative temperature coefficient junction voltage so as to get reduced output voltage variation with respect to temperature.

Figure 2 shows conventional Bandgap reference [4] circuit which employs high op-amp to maintain two node voltages equal so as to create a PTAT voltage across R_2 so as to cause the current through the circuit to be PTAT. Output of the circuit can be written as below.

$$V_{ref} = V_{BE2} + \frac{V_T \ln(n)}{R_2} \cdot (R_3 + R_2) \qquad (2.1)$$

If above equation is differentiated with respect to T and derivative is set to zero at $T = T_r$ (Reference temperature) to obtain the resistor ratio so as to get output, first order independent of temperature. Performance of such circuit is mainly limited by logarithmic temperature dependence of junction voltage, which can be removed by using curvature compensation schemes.

Op-amp input offset, Resistor mismatch, Resistor tolerance, resistance temperature coefficient and current mirror mismatch are typical sources of error in conventional BGR circuit, which tend to increases the output voltage drift as compared to predicted result. Effect of such mismatch needs to be explored so as to improve the performance of circuit.

2.2.Performance metric

The performance of a reference circuit is determined by its variation and by its allowable operating conditions [1]. Main specifications of the reference include temperature drift, quiescent current flow, supply voltage range, output current, power supply rejection ratio (PSRR) and startup time. Temperature drift is measured by temperature coefficient (TC) and it is expressed in parts-per-million per degree Celsius (ppm/°C). It's given by the following equation, where V_{ref} is the reference voltage at reference temperature.

$$TC = \frac{\partial V_{ref}}{\partial T} \cdot \frac{1}{V_{ref}} \cdot 10^6 \tag{2.2}$$

Reference voltage variation due to supply variation is described by line regulation which is given by the change in reference voltage for unit change in supply voltage. Power supply rejection ratio is another quantity which checks the robustness and the stability of the circuit with respect to the random variation subjected to the supply voltage. It should be noted that PSRR refers to small signal response while line regulation refers to large signal response. One common method for improving PSRR of circuit is to add a block which generates a regulated supply voltage for bandgap circuit. Basic functionality of the block is to isolate the noisy and variable supply to bandgap core. Such techniques will be elaborated in PSRR improvement section.

2.3.V_{BE} characteristics

First order compensated voltage references do have higher order temperature dependence. High precision voltage reference tries to remove this higher order dependence as well. Technique for removing higher order temperature dependence of first order voltage reference is typically called curvature compensation or curvature correction technique. An accurate analysis of Temperature effects in I_C-V_{BE} characteristics of BJT is given in [13]. Such analysis is of great importance in design of Bandgap reference and curvature compensation of the same. Relationship proposed in [13] can be written as follows.

$$\hat{V}_{BE}(T) = V_{GOr} + \frac{T}{T_r}\left[V_{BE}(T_r) - V_{GOr}\right] - (\eta - \delta)\frac{kT}{q}\ln\left(\frac{T}{T_r}\right) \quad (2.3)$$

Where V_{GOr} is extrapolated bandgap voltage to 0 K, T_r is reference voltage, η is temperature

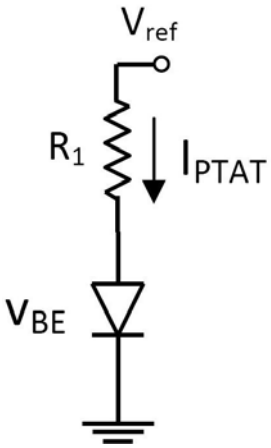


Figure 4 Voltage-mode output structure

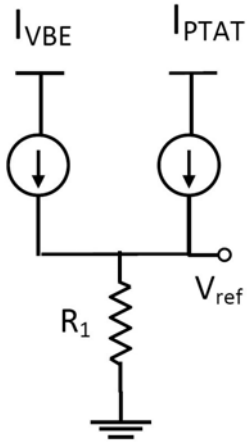


Figure 3 Current-mode output structure

independent constant which ranges from 2 to 4, δ shows temperature dependence of collector current, i.e. if I_C is PTAT then δ is 1 and if it's temperature independent then δ is 0.

2.4.Output stage

A voltage- mode output structure, as the name suggest, sums temperature dependent voltages. The positive TC of PTAT voltage cancels negative TC of forward-baised diode voltage. Voltage-mode output stage is most commonly used technique in reference circuits. Low voltage is important design criteria in both analog and digital systems. As a result voltage-mode output stage is not suitable for low voltage operation as the fundamental limit of the voltage-mode topology is 1.2 V.

A current-mode output topology, as the name suggest, sums the temperature dependent currents. The positive TC of PTAT current cancels negative TC of Complimentary to absolute temperature (CTAT) current. Unlike voltage-mode topology, current-mode topology is flexible enough to allow reference voltages from few milli-volts to few volts. So this topology is more suitable for low voltage operation.

3. LITERATURE SURVEY

3.1.Introduction

Shrinking device dimensions in advancing CMOS technologies require lower supply voltages to ensure device reliability. As a result, analog circuit designers are faced with many challenges in finding new ways to build analog circuits that can operate at lower supply voltages while maintaining performance. Bandgap references are subject to these head-room problems especially when the required supply voltage approaches the bandgap voltage of silicon.

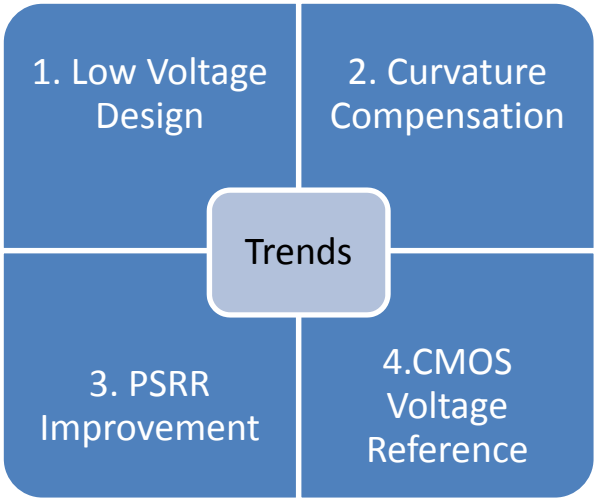


Figure 5 Research trends in voltage reference

There are some applications like high-performance data converters and low-voltage power supply systems that require even more accuracy than what a first-order voltage reference can supply. Consequently, higher-order references—curvature compensated references—are necessary.

The design of complex systems with analog, digital and switched-capacitor building blocks integrated on one chip suffers from large signal variations on the power supply lines. The performance of a system influenced by power-supply variations can be described by the power supply rejection ratio. Thus, it is also necessary to achieve high power supply rejection ratio over broad frequency range in order to reject noise from the high speed digital on chip. Although bandgap voltage reference shows very good performance, it is not the only voltage reference available in CMOS technologies.

3.2.Low Voltage Design

Demand for low-voltage operation is apparent in battery operated mobile products. Conventional BGR circuit's theoretical min $\{V_{DD}\}$ is about 1.4 V. Two factors limit the conventional circuit from operating under 1 volt

a. The reference voltage is around 1.25 V which exceeds 1-V supply
b. The input common-mode voltage of the amplifier.

Various techniques for Sub-1-V operation of conventional BGR circuit is proposed which includes resistive subdivision [14], use of DTMOS transistors [15], use of BiCMOS [7], and use of transimpedance amplifier [16]. Improvement of [14] is proposed in [17] which is now standard low voltage circuit which doesn't require low threshold devices. More recently a fractional bandgap reference was proposed in [18] which increases input common mode voltage of op-amp so as to simplify the op-amp design.

3.2.1. Banba et al. (1999)

In this paper [14] first limiting factor is resolved by scaling the output voltage. So that by choosing reference voltage lower than one volt, the minimum supply voltage can be lowered. This achieved by two resistors at two nodes V_a and V_b.

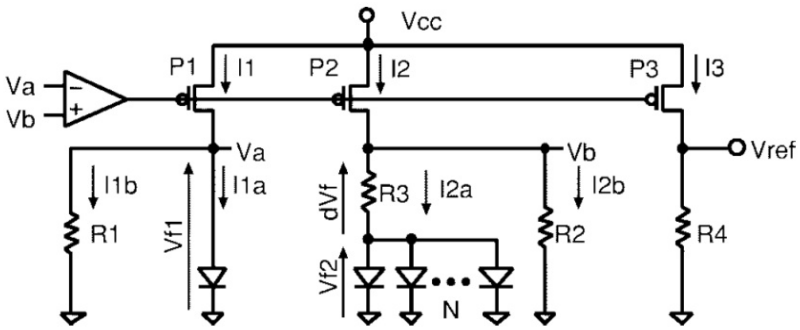


Figure 6 Resistive subdivision Technique

This kind of topology is called current mode because PTAT and CTAT current is added together and then converted to voltage by resistor R4. V_{ref} can be written as follows

$$V_{ref} = R_4 \cdot \left[\frac{V_{f1}}{R_2} + \frac{dV_f}{R_3} \right] = \frac{R_4}{R_2} \cdot \left[V_{f1} + \frac{R_2}{R_3} dV_f \right] \tag{3.1}$$

Where V_{f1} is the voltage across diode and dV_f is the difference between V_{f1} and V_{f2}. Here the Temperature dependence can be cancelled by an appropriate R2/R3 and N and resistor ratio R4/R2 will scale down the bandgap voltage reference to be less than 1.2 V. Vref is set such that VDS1 ≈ VDS2 ≈ VDS3, so as to get good current matching at different temperatures.

3.2.2. Jiang et al. (2000)

In this paper [16] voltage scaling is achieved by using transimpedance amplifier which has low input resistance and high gain. The internal node of the two inputs is set to V_B which is

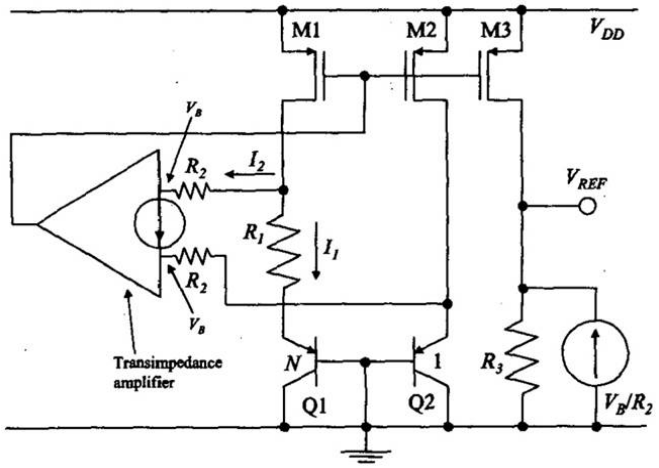


Figure 7 Voltage scaling by transimpedance amplifier

lower than one V_{EB}. So that I_2 also flows in transistors M1, M2 and M3 along with PTAT current. V_{ref} voltage is given by following equation

$$\begin{aligned} V_{REF} &= \left(I_1 + I_2 + \frac{V_B}{R_2} \right) \cdot R_3 \\ &= \left[\frac{V_T \ln(N)}{R_1} + \frac{V_{EB2} - V_B}{R_2} + \frac{V_B}{R_2} \right] \cdot R_2 \\ &= \frac{R_3}{R_2} \cdot \left[V_{EB2} + \left(\frac{R_2}{R_1} \right) \ln(N) \cdot V_T \right] \end{aligned} \tag{3.2}$$

In this design matching of node voltages which is set to V_B is most important otherwise due to mismatch VB term would not cancel and this would lead to nonlinearity in reference voltage. Although reported min V_{DD} is 1.2, this approach has a great potential to further reduce the minimum V_{DD}

3.2.3. Leung et al. (2002)

To reduce input common mode voltage of amplifier a resistor divider is used [17]. Apart from that in order to maintain the operation of amplifier in High-Gain region, source-bulk junctions of all PMOST are forward biased by 0.3 V. DC level shift circuit is also used to maintain the amplifier input transistor in saturation.

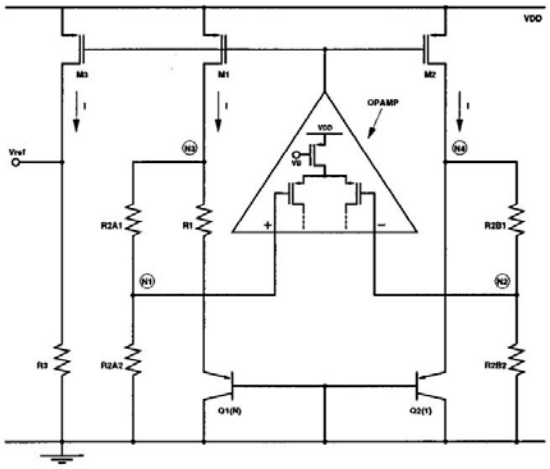


Figure 8 Low voltage technique without low threshold devices.

3.2.4. Perry et al. (2007)

In this paper [18], input common mode voltage is increased by using unity gain buffer and an additional BJT. Benefit of doing so is to relax the design constrains of amplifier. This increases the minimum voltage required but overall better performance is obtained without using forward biased source-bulk junctions and DC level shift amplifier.

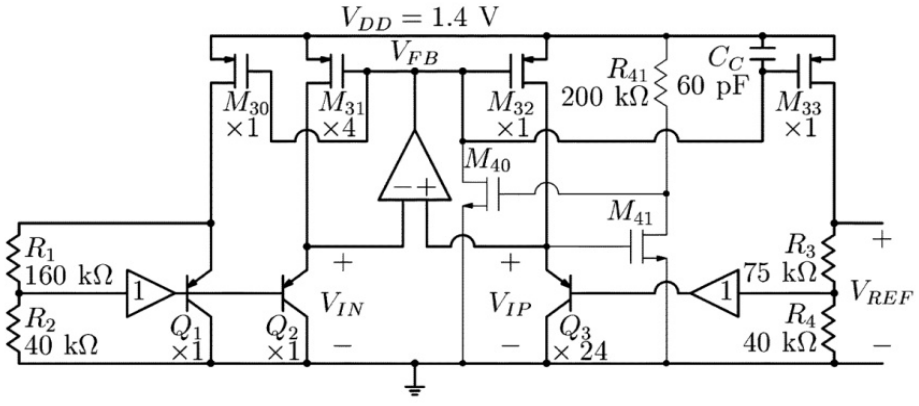


Figure 9 Fractional voltage reference

3.3.Curvature Compensation

Conventional BGR circuit is temperature compensated in first order only. So higher order compensation called quadratic compensation is proposed in [11]. One widely used simple technique is given in [7]. Low voltage BGR circuit has often more temperature dependence then their conventional counterpart. This has resulted in newer curvature compensation techniques such as resistor compensation [6] and matched nonlinear compensation [8], [9].

3.3.1. Malcovati et al. (2002)

Here identical resistor R_5 and R_4 is introduced between two transistor carrying collector current with PTAT and temperature independent nature respectively [7]. Temperature dependence for

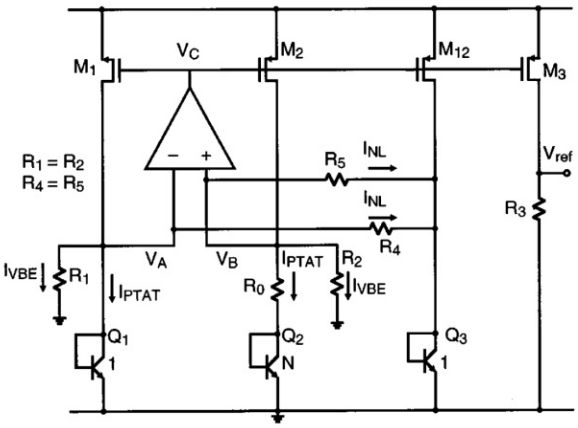


Figure 10 Match nonlinear compensation by Malcovati et al.

V_{BE} was given in section 2.3 where δ was defined to be dependent on temperature dependence of collector current through BJT. For Q3, current is first order independent of temperature so $\delta \approx 0$, For Q2, current is proportional to absolute temperature (PTAT), so $\delta \approx 1$. V_{BE} for Q3 and Q2 is given by following equations.

$$V_{BE3} = V_{GOr} + \frac{T}{T_r}\left[V_{BE}(T_r) - V_{GOr}\right] - (\eta)\frac{kT}{q}\ln\left(\frac{T}{T_r}\right) \tag{3.3}$$

$$V_{BE2} = V_{GOr} + \frac{T}{T_r}\left[V_{BE}(T_r) - V_{GOr}\right] - (\eta - 1)\frac{kT}{q}\ln\left(\frac{T}{T_r}\right) \tag{3.4}$$

$$\Delta V_{BE} = V_{BE2} - V_{BE3} = \frac{kT}{q}\ln\left(\frac{T}{T_r}\right) \tag{3.5}$$

Difference between this two voltages (ΔV_{BE}) forces current through R_4 and R_5, which is proportional to nonlinear term in V_{BE} equation and by appropriate scaling of this term the nonlinear term in the V_{ref} can be removed. Output reference voltage is given on the following equation,

$$V_{ref} = R_3 \cdot \left(I_{PTAT} + I_{VBE} + I_{NL} \right) \tag{3.6}$$

$$\begin{aligned} V_{ref} &= R_3 \cdot \left(\frac{V_T \ln(N)}{R_0} + \frac{V_{BE1}}{R_2} + \frac{V_{BE2} - V_{BE3}}{R_5} \right) \\ &= R_3 \cdot \left(\frac{V_T \ln(N)}{R_0} + \frac{V_{BE1}}{R_2} + \frac{V_T \ln\left(T / T_r \right)}{R_5} \right) \end{aligned} \tag{3.7}$$

By choosing appropriate R_2/R_0 and N, first order dependence is cancelled. While by setting, nonlinear dependence is cancelled.

$$\frac{R2}{R5} = \eta - 1 \tag{3.8}$$

Theoretically, V_{ref} independent of temperature can be obtain by this technique. However, due to the non-ideal PTAT and temperature dependence of resistors it is not always possible. Also errors due to mismatch of current mirror also causes error in reference voltage.

3.3.2. Leung et al. (2003)

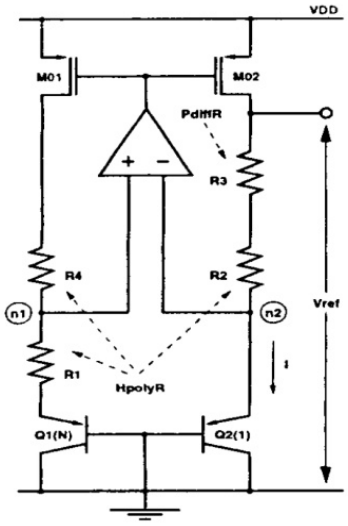


Figure 11 Resistive temperature compenstation

Instead of adding a new structure for creating a non linear term, in this method, by using resistors with having different temperature coefficient, temperature dependent resistor ratio is created [6]. Here both R1 and R2 are made of same material, while R3 is made of high-resistive poly having negative TC. In this case V_{ref} can be given by following equation

$$V_{ref} = V_{EB2} + \left(\frac{R2}{R1}\right)\cdot \ln(N)\cdot V_T + \left(\frac{R3}{R1}\right)\cdot \ln(N)\cdot V_T \tag{3.9}$$

Nonlinear term temperature dependent term in VEB can be expressed into a sum of high-order T terms; high-order temperature-dependence cancellation can be achieved depending on the relative temperature coefficients of R_1 and R_3.

3.3.3. Ker et al. (2006)

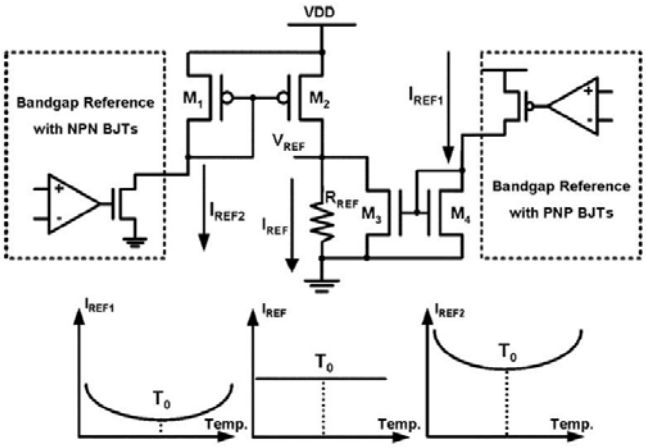


Figure 12 Match nonlinear compensation by Ker et al.

In this technique [8], two types of bandgap reference circuits are used, first with NPN BJTs and with PNP BJTS. Current formed by this two kind of reference I_{REF2} and I_{REF1} are subtracted by using current mirrors to compensate for the high-order temperature-dependence factor of V_{BE}. V_{REF} can be written by following equation.

$$\begin{aligned} V_{REF} &= R_{REF}\left(K_2 I_{REF2} - K_1 I_{REF1}\right) \\ &= R_{REF}\left[\left(\frac{K_2 V_{BE\_pnp}}{R_{1\_npn}} - \frac{K_1 \left|V_{BE\_pnp}\right|}{R_{1\_pnp}}\right) + \frac{kT}{q}\left(\frac{K_2 \ln N_{npn}}{R_{3\_npn}} - \frac{K_1 \ln N_{pnp}}{R_{3\_pnp}}\right)\right] \end{aligned} \tag{3.10}$$

By choosing proper K_2 and K_1 higher order dependence is cancelled. In the above equation the quantity with PNP (NPN) subscript refer to reference with PNP (NPN) BJTs. This technique is useful for high precision application. Output is scaled version of bandgap voltage. Major draw back of the circuit is that it requires parasitic NPN BJT which is not generally available in standard CMOS process.

3.3.4. Qin et al. (2006)

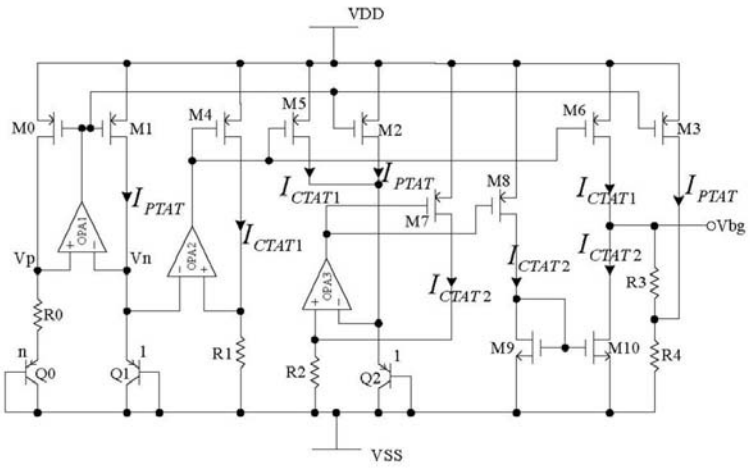


Figure 13 Match nonlinear compensation by Qin et al.

Here Q1, Q2, OPA2, OPA3 generates two CTAT currents, whose difference is taken by current mirror consisting of M9, M10. As the current through Q1 is PTAT and through Q2 is first order temperature independent, by choosing appropriate scalling factors, logarithmic term can be cancelled. Although logarithmic term has been eliminated, the first-order dependence will still exists, which is cancelled by adding an extra PTAT current which is done by M3. Advantage of this technique is that it doesn't need NPN parasitic bipolar which is not often available in standard CMOS process. It should be noted that to make the function of proposed bandgap reference with initiation of the supply voltage bias circuit is needed [9].

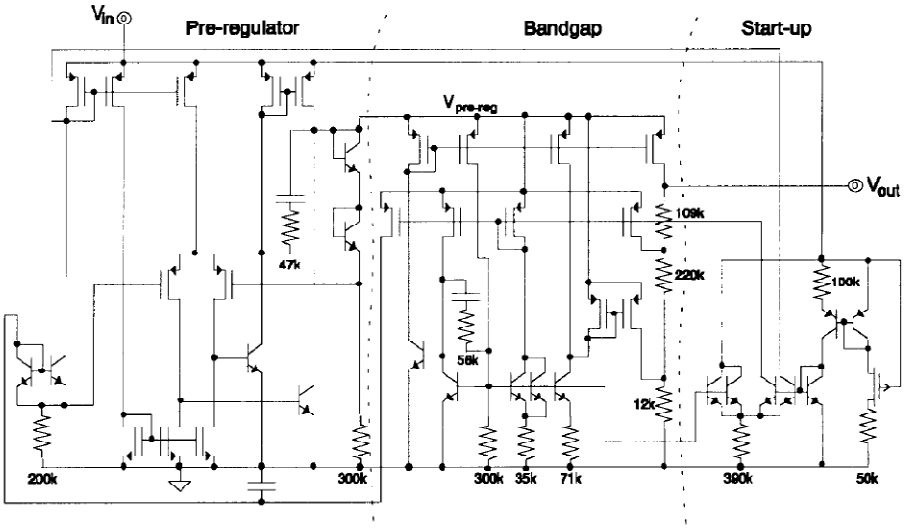


Figure 14 Piecewise linear curvature correction

3.3.5. Rincon-Mora et al. (1998)

In this paper technique of piecewise-linear curvature-correction (Fig. 14) is introduced [12]. The basic idea is to add a correcting nonlinear current over certain temperature range to reduce the temperature variation. Extra circuitry for correction is only a subtractor which gives this technique a distinct advantage as compared to other techniques described previously; also no extra resistors are required so that circuit is also area effective. To reduce the supply voltage variation effect on the bandgap circuit a pre-regulator is also added which generates the V_{pre_reg} voltage. The major disadvantage of this circuit is that it's implemented bipolar technology.

3.4.PSRR Improvement

A pre-regulator circuit which generates internal regulated voltage from which BGR circuit operates is included to improve PSRR [19], [20], [21]. The noisy and variable supply is isolated from the reference by means of a Pre-regulator. The variation of regulated voltage is much lower as compared to supply voltage variation. Typically a Pre-regulator will increase the minimum supply voltage and power consumption. So it's necessary that pre-regulator consumes less power.

3.4.1. Tham et al. (1995)

Here M1, M2, M3, Q1, Q2, R1, R2 consist of conventional BGR circuit, A pre-regulator Feedback Structure constitute of cascode amplifier (M5-M8) and M9. Higher the loop gain of the feedback structure, better the PSRR is achieved. [20]

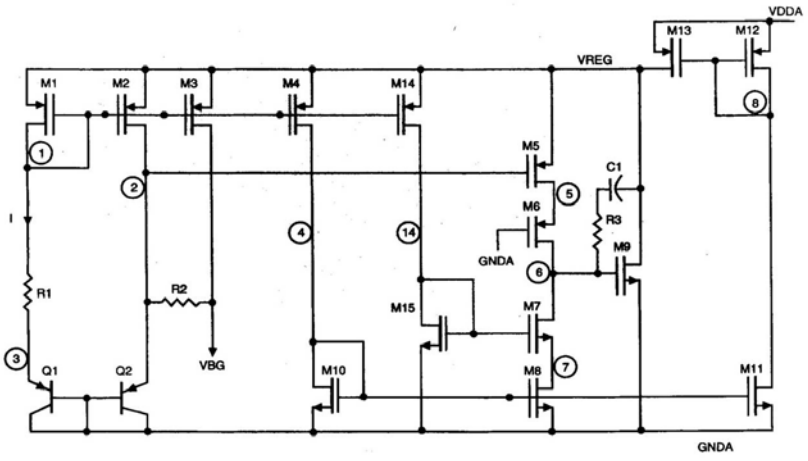


Figure 15 PSRR improvement technique proposed by Tham et al.

3.4.2. Brooks et al. (1994)

In this paper [21], proposed circuit uses a pre-regulator which is essentially a non-inverting amplifier. Output of amplifier A1 is the regulated supply Vrs which drives the bandgap core and rest of the circuits. Reference required for non-inverting amplifier is generated by bandgap circuit. Improvement in the PSRR of whole circuit would be the sum of PSRR of pre-regulator and PSRR of bandgap core. PSRR of Pre-regulator is mainly limited by gain of op-amp. This kind of technique need start-up circuit because operating point of bandgap core depended on pre-regulator and operating points of pre-regulator depends on bandgap core.

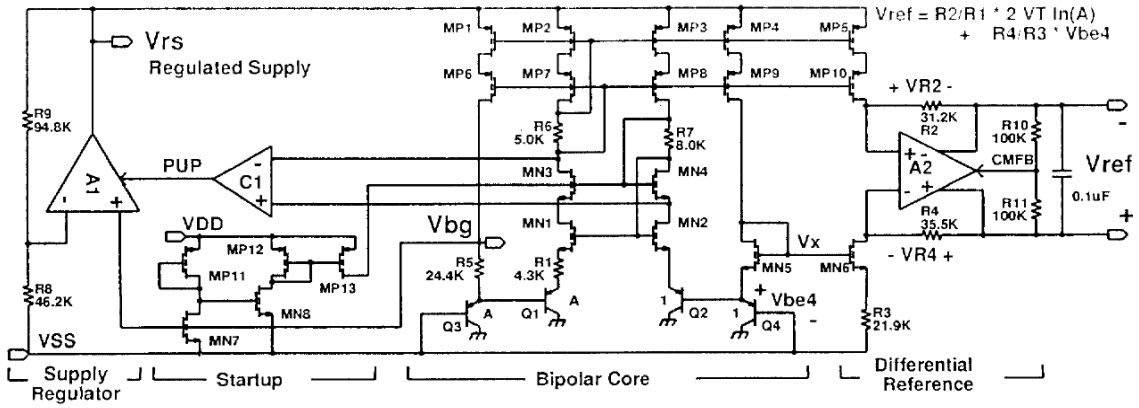


Figure 16 PSRR improvement by using non-inverting amplifier.

3.5.CMOS Voltage Reference

As conventional BGR circuit requires a BJT, which is more often implemented in standard CMOS technology as vertical parasitic BJT having low β and high base resistance, more recently reference circuits, which uses only MOS transistors and which is applicable in low-cost CMOS technology, are proposed. One of the simplest circuit, proposed in [23] which gives output by weighted difference between gate source voltages of MOST. Other techniques either add gate-source voltage [24] or threshold voltage of MOS transistor [25] to thermal voltage to get low temperature dependence.

4. IMPROVED PSRR VOLTAGE MODE BANDGAP REFERENCE

4.1.Introduction

In order to achieve the specification given by STMicroelectronics, A CMOS bandgap voltage reference circuit with 2.7 V is described which generates reference voltage of 1.21 V. It is implemented in 0.18 µm technology with V_{tn} = 0.29 and $|V_{tp}|$=0.42 with a 2.1 mV maximum variation over –25 to 150 °C temperature range with power consumption of 0.9 mW. In order to promote the PSRR performance, the technique proposed in [21] is used. The circuit has a DC PSRR of -105 dB.

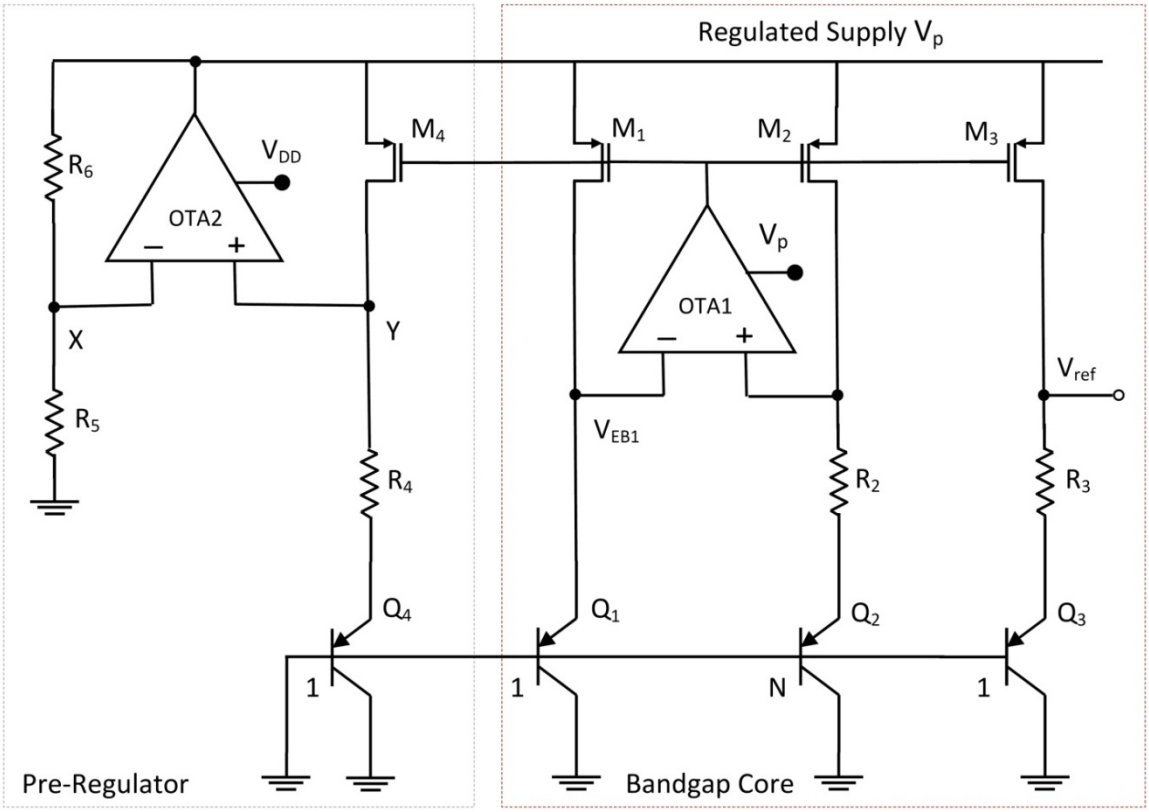


Figure 17 Schematic of improved PSRR BGR circuit

Table 1: BGR Circuit component values			
R2	10 kΩ	R4	130 kΩ
R3	132 kΩ	R5	100 kΩ
R6	23 kΩ	N	8
M1	W = 1 µm , L = 0.18 µm	M2	W = 1 µm , L = 0.18 µm
M3	W = 1 µm , L = 0.18 µm	M4	W = 1 µm , L = 0.18 µm

4.2.Design details

The band gap voltage reference circuit shown in figure 17 using an amplifier with a PMOS input stage is designed [5]. PTAT current generation is done with the help of OTA1 (which has a gain of 68.4 dB). This PTAT current is mirrored by M3 transistor and PTAT voltage is generated across R3 which added to VBE. As PTAT voltage is added to CTAT voltage rather than current this topology is called voltage mode. Conventional voltage mode BGR is chosen because as the required reference voltage is 1.21, voltage mode circuit would be best suited [1].

The input common mode voltage of the Op-Amp is 0.7 V and as the temperature increases this decreases further. This forces us to use an Op-Amp with PMOS input stage noting that an Op-Amp with NMOS input stage can't operate with such a low input common mode voltage. Resistors are planned to be implemented as poly so their temperature coefficient also considered while simulating the circuit. The poly resistor temperature coefficient is taken to be 0.75e-3 /K. Bandgap core and OTA1 operates from a 1.5 V supply

The bandgap core has a DC PSRR of -23.8 dB, which is mainly limited by the open loop gain of OTA1. In order to get the PSRR of -80 dB operational amplifier gain should be around 80 to 100 dB. Which is not possible with simple two stage OTA and also such large gain OTA will lead to stability issue.

In order to improve PSRR of circuit, technique proposed in [21] is used. In this technique the BGR circuit is operated from a regulated voltage generated by a pre-regulator circuit. The pre-regulator circuit consists of non-inverting amplifier which generates 1.5 V from a 1.2 V input at its non-inverting terminal. The input for the pre-regulator block is also generated by an identical structure used in bandgap core. The pre-regulator has a DC PSRR of -81 dB. So the over all PSRR equals the sum of PSRR of BGR core block and PSRR of pre-regulator block. It comes out to be -105 dB.

Both OTA1 and OTA2 are two stage amplifiers, each having a differential amplifier as the first stage and a common source amplifier as the second stage. In order to get good phase margin miller compensation is used. Table 2 shows the features of designed Op-Amps.

Table 2: OTA features		
Parameter	OTA1	OTA2
Gain	68.4 dB	66.6 dB
Gain-Bandwidth product	2.5 MHz	18 MHz
Phase Margin	66 °	67 °
Supply Voltage	1.5	2.7
Power	30 µW	939 µW

The major difference between the two Amplifiers is the amount of current they are able to supply and supply voltage they operate at. As OTA1 is driving the gate node of a MOS transistor, OTA1 doesn't need to supply any output current. While OTA2 is used in a non-inverting configuration so there is resistive loading, and also, it has to supply the current required for the BGR circuit and the OTA1.

During the initial design, the length of all MOS transistors in the OTA were minimum i.e. 0.18µm. In that case the OTA was only able to give a maximum gain of about 50 dB, which was inadequate to get a good PSRR. So both OTAs were redesigned with a larger length (2 µm) to get good gain and less channel length modulation.

4.3.PSRR analysis

In general, any electrical circuit has an input, an output, and a power node. If the transfer function from input node to output node is called the open-loop transfer function or gain (A), and the transfer function of the power node to the output node is called the power supply gain (A_P), the power supply rejection ratio (PSRR) is defined as ratio of gain (A) to power gain (A_P). As for bandgap voltage reference, as there is no input node, PSRR for BGR is same as power gain (A_P). [27].

Detailed frequency analysis of PSRR in Brokaw bandgap is given in [26] where PSRR is derived as function of frequency by using small signal analysis. Such approach of using small signal analysis for calculating PSRR is useful for small cell such as Brokaw cell where no Opamp is used, but it becomes tedious when multiple paths exist from supply node to output node; it becomes very difficult to analyze the whole circuit. In this analysis more intuitive approach is used so that the effect of each block can be analyzed on the PSRR of the whole circuit.

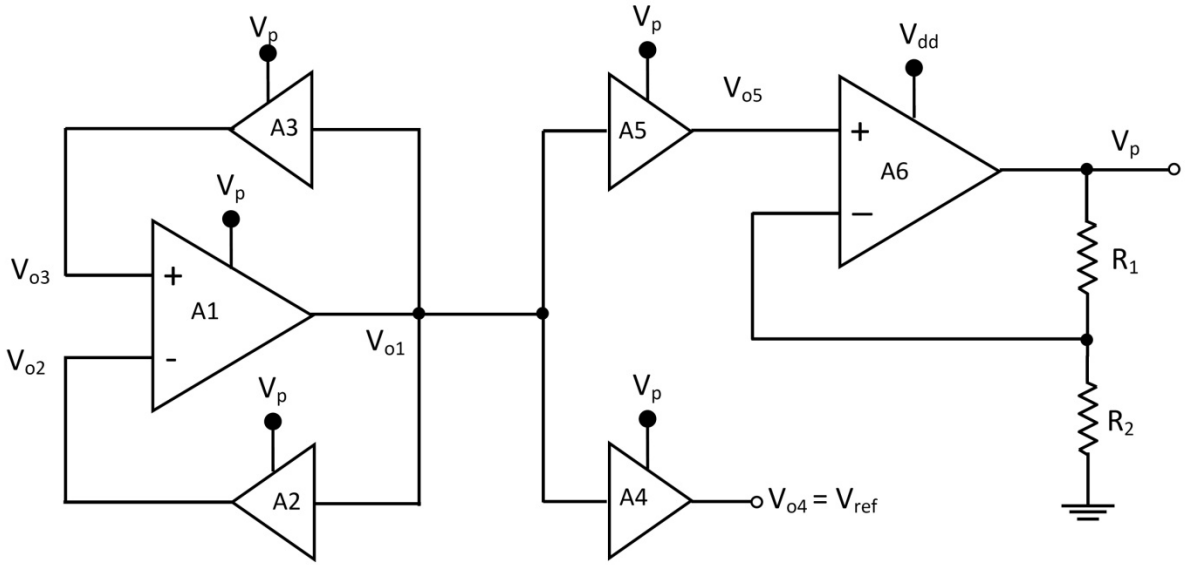


Figure 18 Equivalent circuit for PSRR calculation

In order to simplify the problem, an approach is used to divide the whole circuit, as shown in Fig.16, in the sub-block and all the sub-blocks are characterized by their gain (A) and power gain (A_P), now problem remain to define a relation between the PSRR and gain and power gain of all the blocks. In above figure i^{th} block has gain of A_i and power gain of A_{pi}. Now we can write V_{o1} in terms of A_1, A_{P1} and its input node voltages V_{o2} and V_{o3}.

$$V_{o1} = A_1\left(V_{o3} - V_{o2}\right) + A_{p1}V_p \tag{4.1}$$

Similarly for A2 and A3 Blocks,

$$V_{o3} = A_3V_{o1} + A_{p3}V_p \tag{4.2}$$

$$V_{o2} = A_2V_{o1} + A_{p2}V_p \tag{4.3}$$

Finally the V_{ref} can be written as,

$$V_{o4} = V_{ref} = A_4V_{o1} + A_{p4}V_p \tag{4.4}$$

By combining equation 4.1, 4.2, 4.3 and 4.4, relation between V_{o4} and V_p can be derived.

$$\frac{V_{o4}}{V_p} = A_{p4} + \frac{A_4 A_{p1} + A_4 A_1 \left(A_{p3} - A_{p3}\right)}{1 + A_1 \left(A_2 - A_3\right)} = C_4 \tag{4.5}$$

As A4 and A5 blocks are identical, gain from V_{o4} to V_p and V_{o5} to V_p will be equal. For non-inverting amplifer (A6) V_p can be written as

$$V_p = A_6 \left(C_4 V_p - \beta V_p\right) + A_{p6} V_{dd} \tag{4.6}$$

Where β is defined as $R_2/(R_1+R_2)$ and C4 is given by Equation 4.5. By combining Equation 4.5 and 4.6 PSRR can be written as

$$PSRR = \frac{V_{ref}}{V_{dd}} = \frac{V_{o4}}{V_{dd}} = \frac{V_{o4}}{V_p} \cdot \frac{V_p}{V_{dd}} = \frac{C_4 A_{p6}}{1 + A_6 \left(\beta - C_4\right)} \tag{4.7}$$

By using small signal analysis, gain and power gain of each block can be written in term of g_m and r_o of transistors or we can find the gain and power gain of such block in terms of frequency which will enable us to study frequency response of PSRR for BGR circuit. Here analysis is shown for dc case. Table 3 shows such analysis for A2, A3 and A4 blocks. Analysis is straight forward as feedback structure behaves either as common gate amplifier when finding gain from

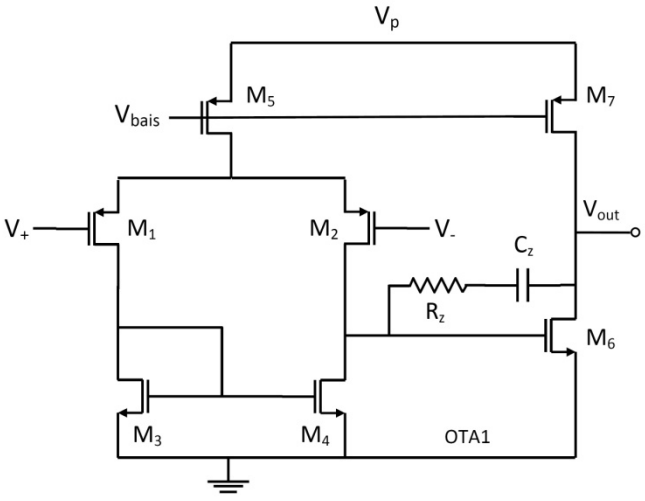


Figure 19 Schematic of OTA1 and OTA2

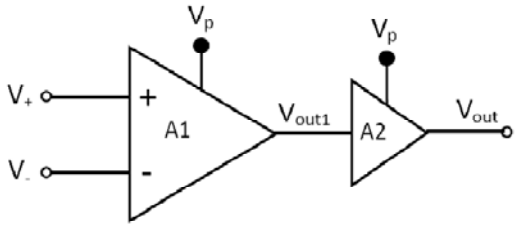


Figure 20 Equivalent circuit of OTA for PSRR calculation

input node to output node or as common source amplifier when finding gain from power supply node to output node. Now calculation of gain and power gain for OTA is given. Fig. 20 shows the schematic for OTA1 and OTA2 used. OTA is characterized by differential amplifier with current mirror load (A_1) block and common source amplifier (A_2) block. Fig. 19 shows the equivalent circuit of OTA for PSRR calculation.

From Fig 19, V_{out1} and V_{out} can be written as

$$V_{out1} = A_1(V_+ - V_-) + A_{p1}V_p \tag{4.8}$$

$$V_{out} = A_2 V_{out1} + A_{p2}V_p \tag{4.9}$$

By combining Equation 4.8 and 4.9 V_{out} can be written as

$$V_{out} = A_2 A_1 V_{in} + (A_{p2} + A_2 A_{p1}) \cdot V_p \tag{4.10}$$

Coefficient of V_{in} in Equation 4.10 is overall gain of Opamp and Coefficient of V_p is power gain of Opamp. It can be shown that for Opamp A_1, A_2 A_{p1}, A_{p2} is given by following equations.

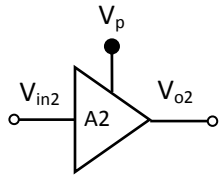
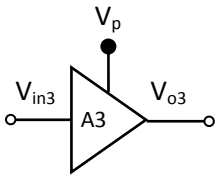
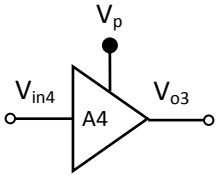
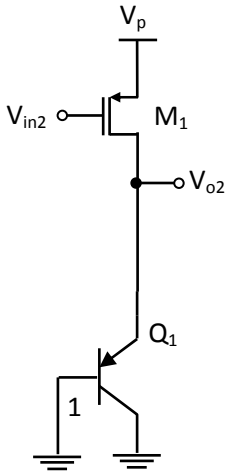
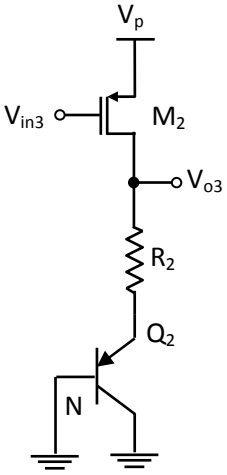
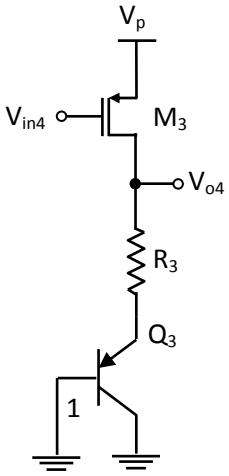
$$A_1 = \frac{g_{m1,2}}{g_{o1,2} + g_{o3,4}} \tag{4.11}$$

$$A_2 = \frac{-g_{m6}}{g_{o6} + g_{o7}} \tag{4.12}$$

$$A_{p1} = \frac{(g_{m1} + g_{o1}) \cdot (g_{m5} + g_{o5})}{[(2g_{m1} + 2g_{o1}) \cdot (g_{m3} + g_{o3})] + [g_{o5} \cdot (g_{m3} + g_{o3} + g_{o1})]} \tag{4.13}$$

$$A_{p2} = \frac{g_{m7} + g_{o7}}{g_{o6} + g_{o7}} \tag{4.14}$$

Table 3: Gain and Power gain of A2, A3 and A4 blocks in terms of g_m and r_o

		
		
$A_2 = \left.\frac{v_{o2}}{v_{in2}}\right\|_{v_p=0} = \frac{-g_{m1}}{g_{mq1}+g_{o1}}$	$A_3 = \left.\frac{v_{o3}}{v_{in3}}\right\|_{v_p=0} = \frac{-g_{m2}}{\left(R_2+g_{mq2}^{-1}\right)^{-1}+g_{o2}}$	$A_4 = \left.\frac{v_{o4}}{v_{in4}}\right\|_{v_p=0} = \frac{-g_{m3}}{\left(R_3+g_{mq3}^{-1}\right)^{-1}+g_{o3}}$
$A_{p2} = \left.\frac{v_{o2}}{v_p}\right\|_{v_{in2}=0} = \frac{g_{m1}+g_{o1}}{g_{mq1}+g_{o1}}$	$A_{p3} = \left.\frac{v_{o3}}{v_p}\right\|_{v_{in3}=0} = \frac{g_{m2}+g_{o2}}{\left(R_2+g_{mq2}^{-1}\right)^{-1}+g_{o2}}$	$A_{p4} = \left.\frac{v_{o4}}{v_p}\right\|_{v_{in4}=0} = \frac{g_{m3}+g_{o3}}{\left(R_3+g_{mq3}^{-1}\right)^{-1}+g_{o3}}$

4.4.Simulated Results

Table 4 shows the performance summary for the designed BGR Circuit. The circuit operates from 2.7 V while OTA1 and the BGR core operate from the regulated supply voltage which is 1.5 V

Table 4: Performance Summary for improved PSRR BGR	
Power supply voltage (V_{DD})	2.7 V
Technology	0.18 µm
Power Consumption	0.9 mW
Reference Voltage @ T= 27 °C	1.21 V
Maximum Output variation	2.1 mV (-25 to 125
PSRR @ DC	-105.1 dB
@ 1kHz	-102.8 dB
@ 10 kHz	-86.3 dB
@ 100 kHz	-62.9 dB

Figures 21 and 22 show the Vref and Vp variation with respect to temperature. Even though the regulated supply voltage does have temperature dependence, but due to the very high gain of the Op-Amp used in the PTAT loop, the effect of such variation on Vref variation is negligible.

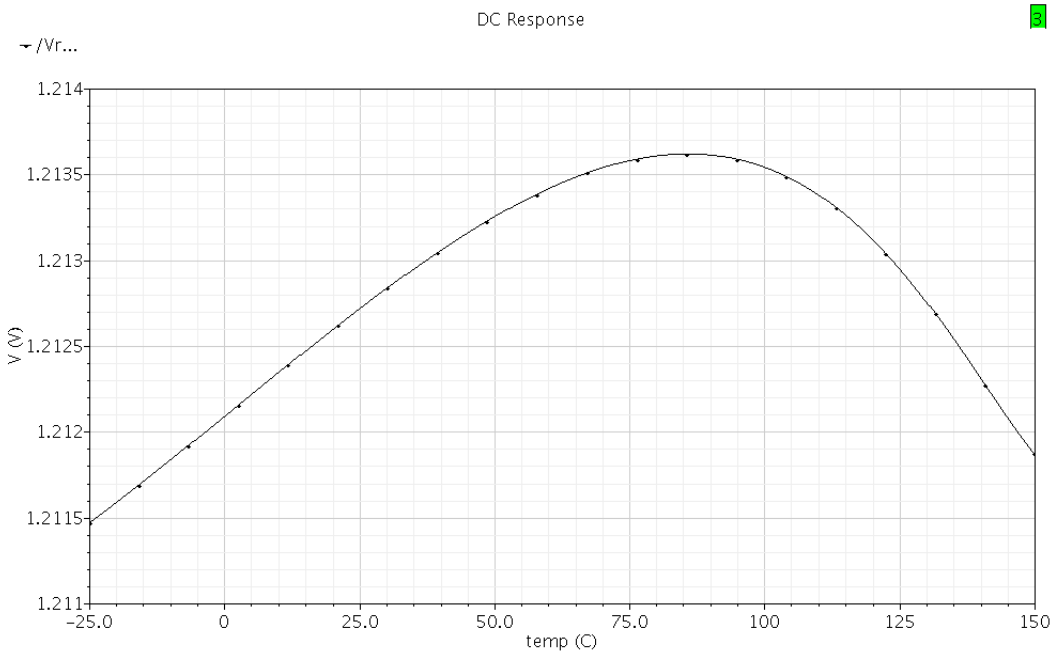


Figure 21 Reference voltage variation with respect to temperature

Figure 23 shows the PSRR of BGR Core, pre-regulator and BGR circuit.

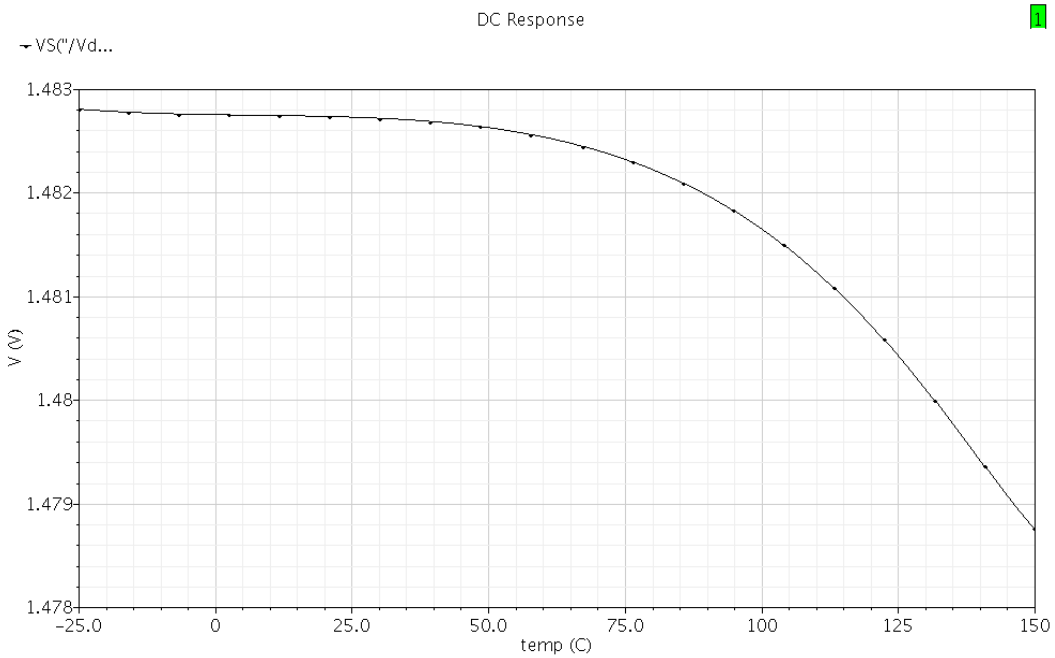


Figure 22 Regulated voltage supply (Vp) variation with temperature

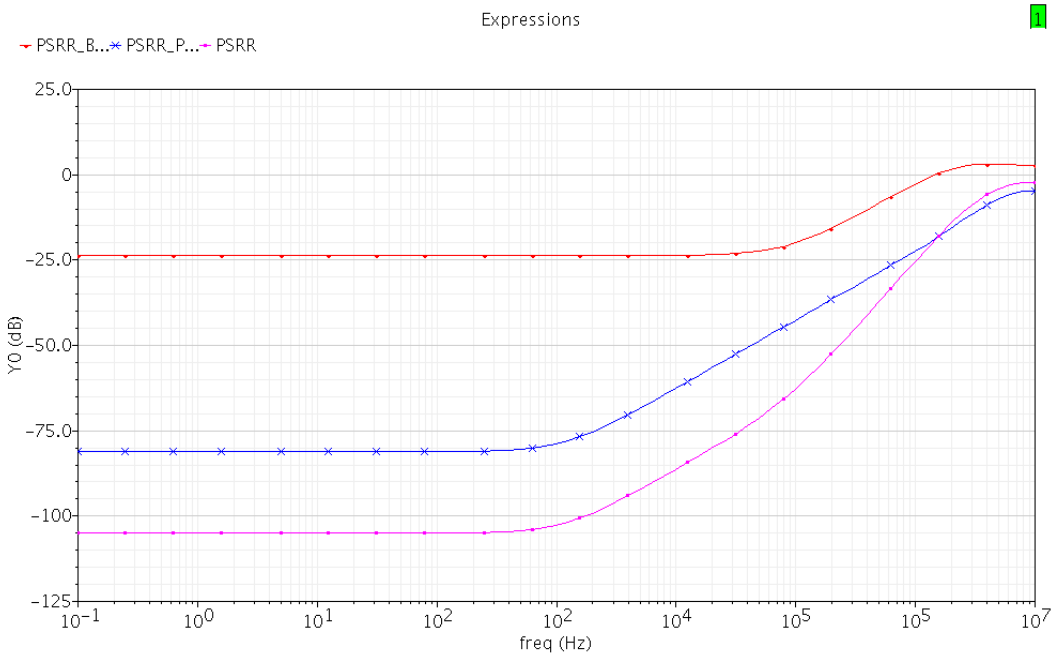


Figure 23 PSRR of bandgap core (RED), pre-regulator (BLUE) and PSRR of BGR (PURPLE).

PSRR value of BGR is calculated by the analyzing technique based on the sub circuit presented in section 4.3. Value of PSRR by hand calculation has excellent agreement with the value observed on simulation. PSRR of bandgap core can still be improved if reference voltage can be taken from inside the feedback loop consisting of OTA1. Then again, circuit would still require pre-regulator to achieve -80 dB PSRR.

The circuit has been successfully verified for threshold voltage variation of ± 50 mV around nominal value, ± 10 % variation of supply voltage and ± 5 % variation of resistance variation. The effect of supply variation is negligible on reference voltage as supply is regulated. Similarly as the BGR operates from supply voltage of 2.7 V circuit is able to handle threshold voltage variation as the VDS of transistors are set to about 100 mV to 200 mV.

5. PIECEWISE-LINEAR CURVATURE-CORRECTED CURRENT MODE BGR

5.1.Introduction

This chapter describes a CMOS bandgap reference which uses piecewise-linear curvature compensation scheme for second order correction. In standard 0.18µm CMOS process, the reference, with 1.8 V supply produces an output of about 928 mv, which varies by 400 µV from -25 °C to 150°C. It dissipates 150 µW and has a DC PSRR of -46 dB.

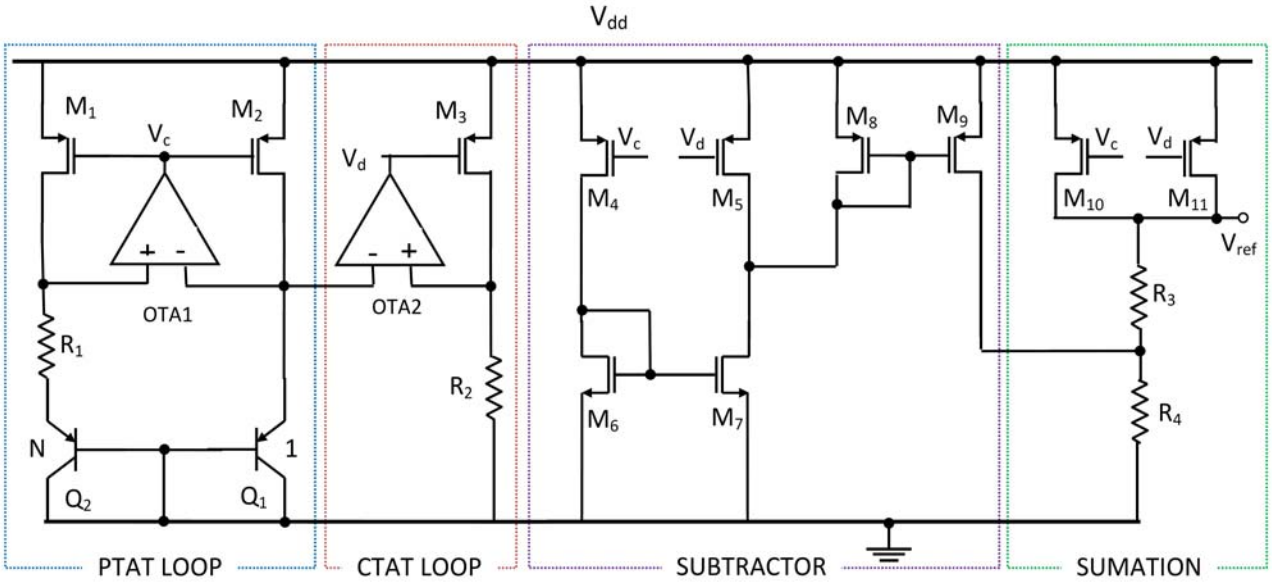


Figure 24 Schematic of proposed circuit

5.2.Curvature Correction method

VBE is nonlinear function of Temperature [13]. So first order BGR reference exhibits higher order temperature dependence, due to which output reference voltage exhibits curvature. To remove this higher order temperature dependence, nonlinear component is added to output.

First order voltage reference would be generated such that its TC is zero at room temperature. But as temperature varies, typical first order compensated reference voltage would varies with temperature as shown in fig. 27(b) by curve for C = 0. Piecewise-linear correction tries to reduce the temperature dependence over a certain portion of temperature range over which the circuit operates.

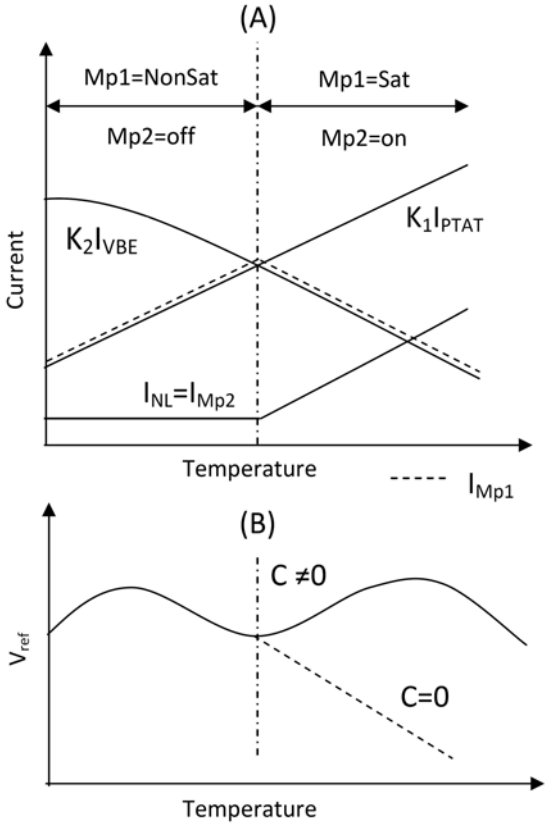


Figure 27 Temperature dependence of non-linear current

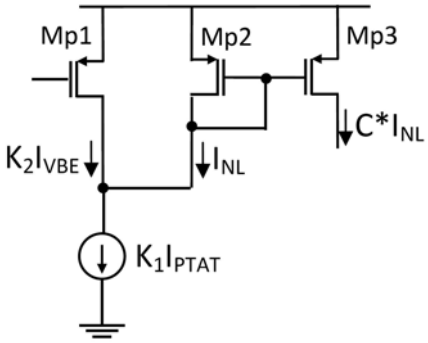


Figure 25 Nonlinear current generation circuit.

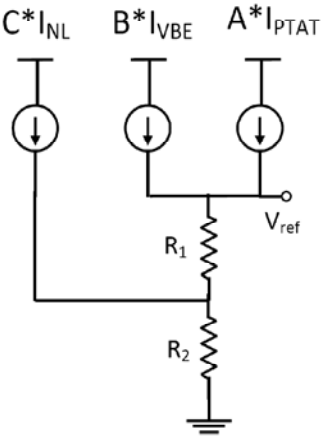


Figure 26 Mixed mode architecture.

The nonlinear component for correction is realized by generating I_{NL} in the current-mode topology of the circuit shown in fig. 25, which essentially performs a current subtraction over the temperature range for which K_1I_{PTAT} is greater than K_2I_{VBE}. Fig. 27 graphically illustrates the operation of the circuit throughout the temperature range. For the lower half of temperature range, where the PTAT current is less than the supplied I_{VBE}. As result, MP2 is off and Mp1 operates in linear region and follows I_{PTAT}. For the upper half of temperature range, however, I_{PTAT} becomes larger than I_{VBE} and consequently, MP1 gets saturated and supplies I_{VBE}, while current through mp2 is difference between K_1I_{PTAT} and K_2I_{VBE}.

Nonlinear current through MP1 is shown in fig. 27 with dashed line. The resulting current in MP2 is nonlinear, off during the first half of the temperature range and on during the latter half. Nonlinear current can be expressed by

$$\begin{aligned} I_{NL} &= 0, && \mathrm{I_{BE}} \geq I_{PTAT} \\ &= K_1 I_{PTAT} - K_2 I_{VBE}, && \mathrm{I_{BE}} \prec I_{PTAT} \end{aligned} \tag{5.1}$$

Where K_1 and K_2 are the constatns defined by current mirror transistors. Finally curavture correction is achieved by combining this thre temperature dependent currents. Curve for $C \neq 0$ in Fig 27(b) shows the compensated reference voltage. It should be noted that relative magniture of nonlinear current is much smaller than I_{PTAT} and I_{VBE}.

Either current mode or voltage mode BGR structure can be used for combining this three currents. As shown in Fig. 26 this nonlinear current is converted to voltage by resistor R_2. We could have added this nonlinear current to R_1, but this kind of mixed mode architecture allows much flexibility for temperature compensation. The resultant relation of the reference votlage (V_{ref}) can be described by

$$V_{ref} = \left(AI_{PTAT} + BI_{VBE}\right)\left(R_1 + R_2\right) + CI_{NL}R_2 \tag{5.2}$$

For the lower temperature range the output is essentially a first order bandgap, while for higher temperature, its piecewise-linearly corrected.

5.3.Design Details

Figure 5 shows the simplified schematic of the bandgap reference. BI_{VBE} AND AI_{PTAT} is implemented by the circuit highlighted by CTAT loop and PTAT loop respectively. N is the area ratio of the BJT between Q_2 and Q_1 and it is set to 8

$$I_{PTAT} = \frac{V_T \ln\left(N\right)}{R_1} \tag{5.3}$$

With the help of the OTA1 the difference between the two base emitter voltage of Q_1 and Q_2 appears across resistor R_1 and it can be shown that this voltage is of PTAT nature. This voltage causes the current through R_1 and therefore the current through M_1 to be PTAT. This current is given by equation 4 where V_T is thermal voltage.

Similarly OTA2 forces base emitter voltage of Q_1 to come across R_2, Which causes current through M_3 to be CTAT. This current is given by equation 5.4

(5.4)

$$I_{CTAT} = \frac{V_{BE}}{R_2}$$

Summing PTAT and CTAT currents generates first order temperature independent current which is done by the mirroring transistor M_{10} and M_{11} and piecewise linear curvature correction is achieved by subtractor circuit. It should be noted that both OTA1 and OTA2 are completely identical. To reduce the channel length modulation long length transistor are

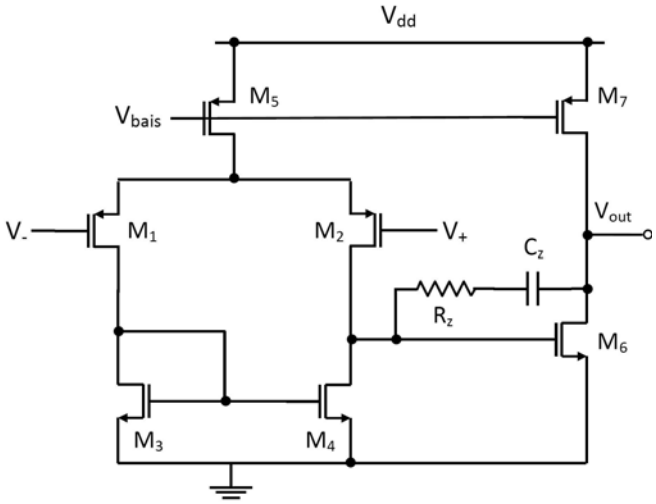


Figure 28 OTA scheme used for proposed circuit

recommended.

Figure 28 shows the Opamp schematic. The Opamp in the BGR circuit is a typical two stage OTA. Transistors $M_1 - M_5$ form a differential pain with current mirror load. Transistor M_6- M_7 forms a common source amplifier. Rz and Cz ensures the stability of the opamp circuit. The operation amplifier was designed using a 0.18um standard CMOS technology. Its simulated features are summarized in Table I.

5.4.Simulated Results

The proposed bandgap reference circuit is designed in standard 0.18 μm CMOS technology. Simulation has been carried out using Cadence Spectre. Threshold Voltage for NMOS and PMOS transistors is 0.29 V and -0.42 V Respectively. Models of MOS and PNP transistors are BSIM3V3.

Table 5: Performance summary for curvature corrected circuit	
Parameter	Value
Power supply Voltage	1.8 V
Technology	0.18 µm
Power Consumption	158.6 µW
Reference voltage at T= 25 °C	928 mV
Temperature Variation (-25 °C to 150 °C)	
Without curvature correction	1.2 mV
With curvature correction	160 µV
DC PSRR	-46.7 dB

The simulated results are tabulated in Table 5. Fig. 29 shows the variation of the reference voltage with temperature over the range of -25 °C to 150 °C. The output reference voltage is 928 mV, and the variation of the output voltage with the curvature correction is 160 µV and without the curvature correction, it is 1.2 mV.

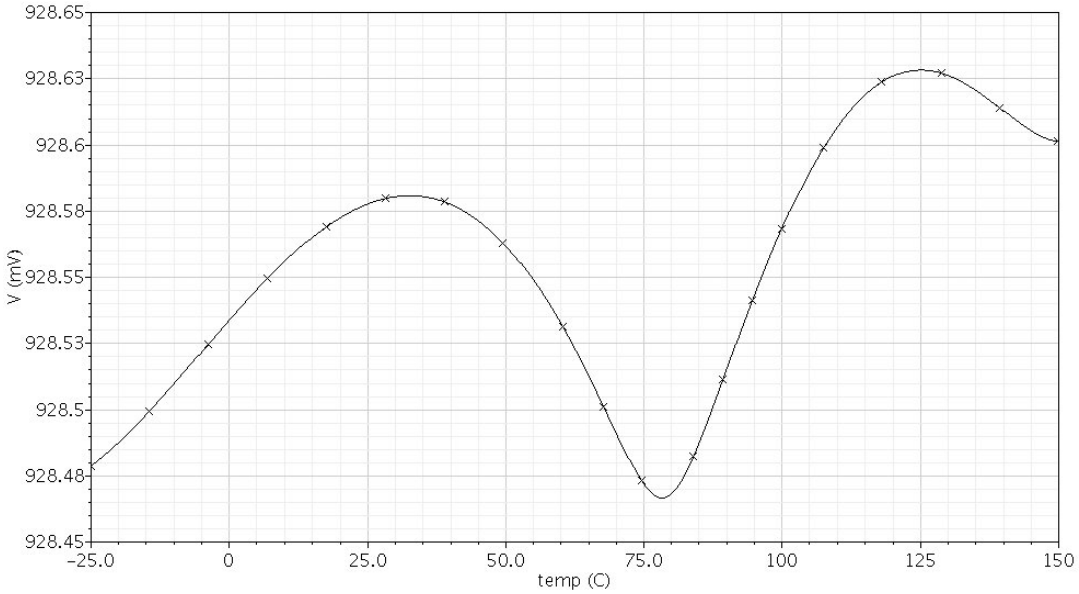


Figure 29 Reference voltage as a function of temperature with curvature compensation.

The minimum V_{DD} for the proposed BGR is 1.6 V. Fig. 30 shows a plot of the gain from the power supply to the reference output versus frequency when VDD varies by 5mV peak to peak and has an average value of 1.8 V. The measured supply gain at DC is -46.7 dB.

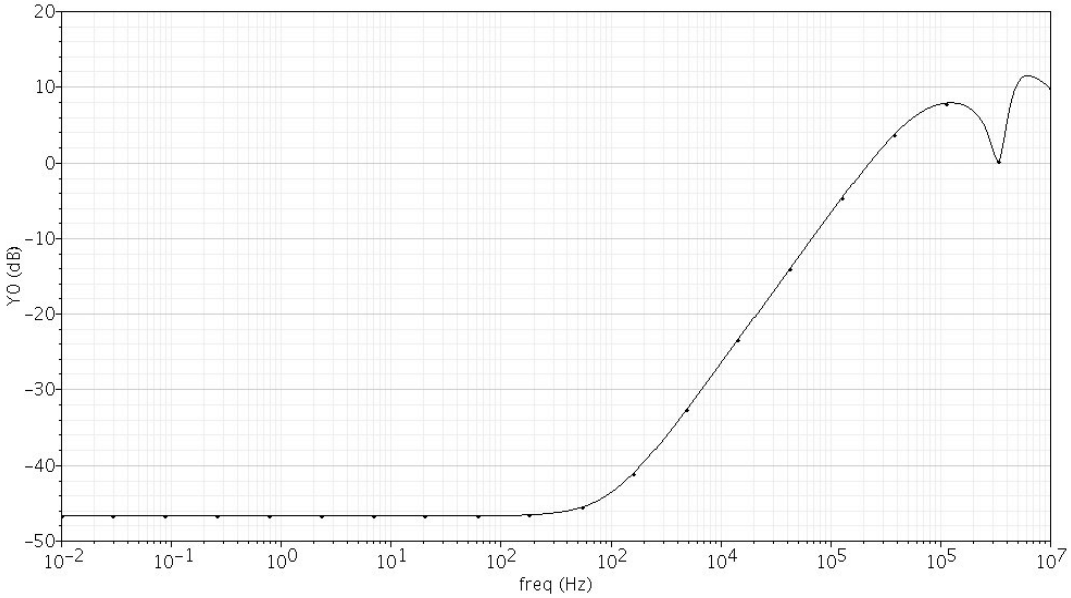


Figure 30 Gain from the power supply to the output versus frequency when V_{DD} varies by 5 mV and has an average value of 1.8 V

Fig. 31 Shows reference voltage as a function of supply voltage. The output voltage will have 0.8mV variation with the supply voltage from 1.6 V to 2.2 V. The power dissipation is 158 µW from a 1.8 V supply.

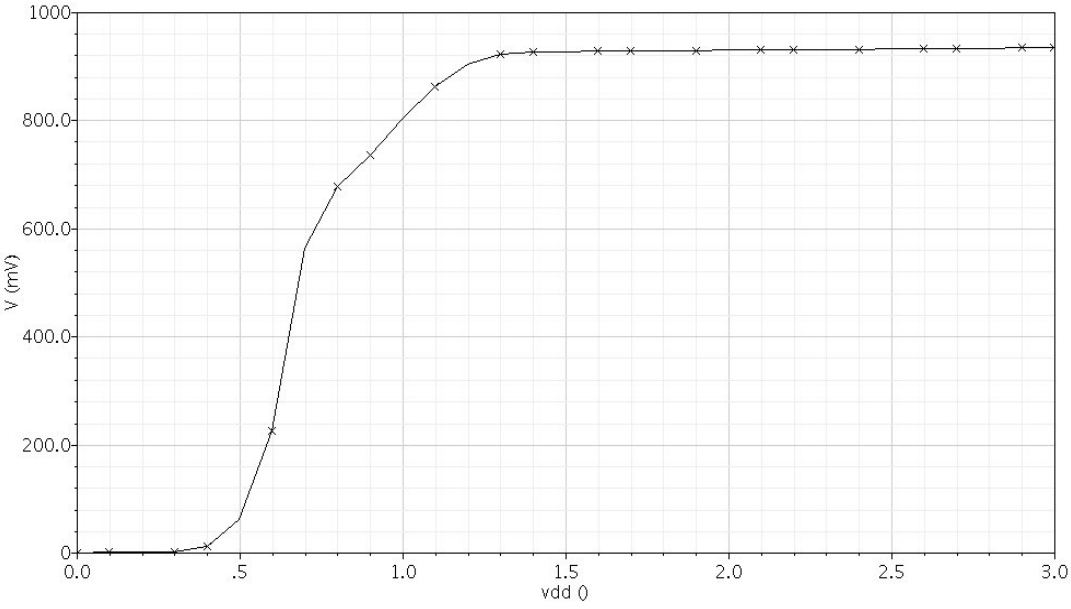


Figure 31 Reference voltage as a function of supply voltage

Fig. 32 shows the effect of supply voltage variation on reference voltage. Topmost curve is for supply voltage of 1.98 V, middle curve is for supply voltage of 1.8 V and bottom most curve is

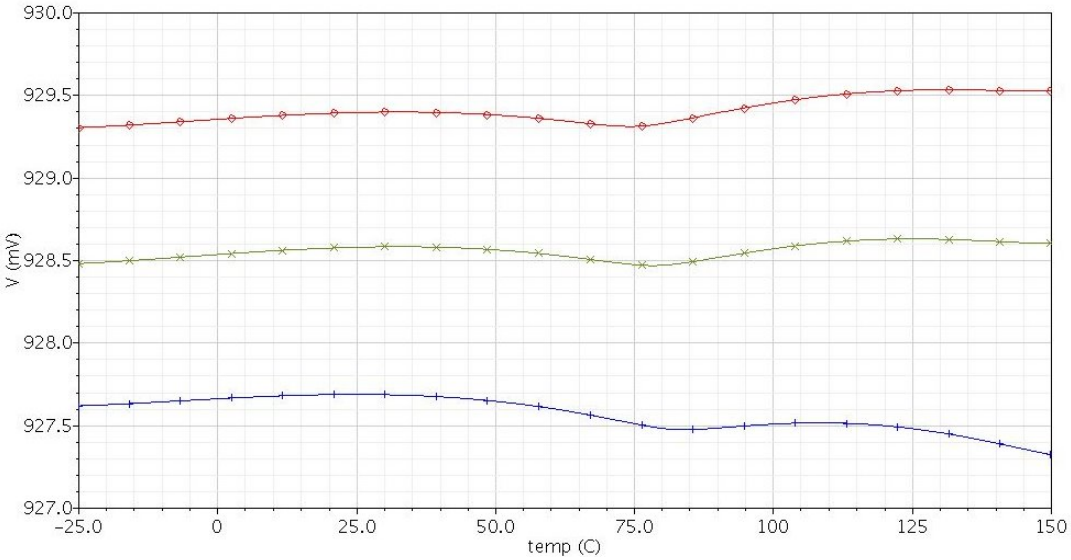


Figure 32 Effect of supply voltage variation of reference voltage.

for supply voltage of 1.62 V. It can be seen that the relative magnitude of second peak in the graph varies for different supply voltages. As the supply varies the first order reference voltage varies and with mismatch of slope between nonlinear correcting term and first order reference second peak tends to shift.

The circuit has been successfully verified for threshold voltage variation of ± 50 mV around nominal value and corresponding reference variation is within ± 150 µV. Circuit has also been verified for the ±10 % supply variation and 5 % resistance variation. Effect of supply variation can reduce by regulating supply voltage with help of pre-regulator. In the end, there exists a tradeoff for PSRR performance and power consumption and silicon area. Minimum supply voltage also tends to increase with the presence of pre-regulator.

6. CONCLUSION

In this work, two bandgap reference circuits were presented. The first circuit is designed to have very high power supply rejection ratio which is an improved PSRR first order bandgap voltage reference with V_{ref} of 1.21 V and PSRR of -102 dB at 1 KHz. The second circuit has a very good temperature performance which is a piecewise-linear curvature compensated bandgap voltage reference with V_{ref} of 928 mV and variation of only 160 μV. Circuit is compatible with CMOS technology and with low voltage operation. The curvature correction circuitry is simple and compact, and easy trimming procedure is possible by the used of mixed mode architecture.

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APPENDIX A: BGR SPECIFICATION

The specs follow:

[It is suggested that the initial research be done with any available MOSIS Specs so as not to hit any Confidentiality snags]

Parameter Minimum Typical Maximum Unit
Supply Vdd-10% Vdd Vdd+10% V

Junction Temperature -25 150 °C
Area TBD mm2
Startup Time 2 us
Output Voltage (Vref=Vbg) 1.21 V
Output voltage (Vref) spread (peak to peak) 30 mV
DC PSRR (Vref) -80dB
Unity Gain Bandwidth 1.0 MHz.

Startup Time : This is the time the circuit will take after PD changes it's state from logic 0 to logic 1 (after the supply has reached it's full value), to generate the output voltage and current within +/-1% of the final value

The circuit should be validated for following conditions:
N-MOS : SLOW, TYP, FAST
P-MOS : SLOW, TYP, FAST
Resistor : TYP-20%, TYP, TYP+20%

APPENDIX B: DEVICE SIZES

Improved PSRR BGR (Fig. 17)			
R2	10 kΩ	R4	130 kΩ
R3	132 kΩ	R5	100 kΩ
R6	23 kΩ	N	8
M1	W = 1 µm , L = 0.18 µm	M2	W = 1 µm , L = 0.18 µm
M3	W = 1 µm , L = 0.18 µm	M4	W = 1 µm , L = 0.18 µm

OTA1 (Fig. 17)			
M1	W = 20 µm , L = 2 µm	M2	W = 20 µm , L = 2 µm
M3	W = 10 µm , L = 2 µm	M4	W = 10 µm , L = 2 µm
M5	W = 40 µm , L = 1 µm	M6	W = 9 µm , L = 2 µm
M3	W = 35 µm , L = 2 µm	R_Z	5 kΩ
C_Z	5 pF		

OTA2 (Fig. 17)			
M1	W = 20 µm , L = 1 µm	M2	W = 20 µm , L = 1 µm
M3	W = 15 µm , L =5 µm	M4	W = 15 µm , L = 5 µm
M5	W = 36 µm , L = 5 µm	M6	W = 29 µm , L =1 µm
M3	W = 30 µm , L = 1 µm	C_Z	2 pF

Piece-wise Linear curvature correction BGR (Fig. 24)			
R1	10 kΩ	R2	109 kΩ
R3	80 kΩ	R4	2 kΩ
N	8	M11	W = 10 µm , L = 5 µm
M1	W = 10 µm , L = 5 µm	M2	W = 10 µm , L = 5 µm
M3	W = 10 µm , L = 5 µm	M4	W = 10 µm , L = 5 µm
M5	W = 6 µm , L = 5 µm	M6	W = 15 µm , L = 5 µm
M7	W = 6 µm , L = 5 µm	M8	W = 10 µm , L = 5 µm
M9	W = 5 µm , L = 5 µm	M10	W = 10 µm , L = 5 µm

Note: OTA1 and OTA2 in Fig. 24 are identical Opamps. Their device sizes are same as OTA1 in Fig 17.

APPENDIX C: BSIM3 MODEL CARD

```
//  Abstract: TSMC 0.18u CMOS018/DEEP (6M, HV FET, sblock) Spectre Models
// simulator options
simulator lang=spice insensitive=yes
//  4-Terminal NMOS Model

.model nmos1 bsim3v3 type=n
+VERSION = 3.1            TNOM    = 27             TOX     = 4.5E-9
+XJ      = 1E-7           NCH     = 2.3549E17      VTH0    = 0.2966698
+K1      = 0.482494       K2      = -0.0118737     K3      = 1E-3
+K3B     = 5.0195709      W0      = 1E-7           NLX     = 2.443731E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.6100514      DVT1    = 0.2724406      DVT2    = -0.1878828
+U0      = 273.8484866    UA      = -1.525788E-9   UB      = 2.786859E-18
+UC      = 4.943779E-11   VSAT    = 9.768529E4     A0      = 0.9881723
+AGS     = 0.1424763      B0      = 6.152611E-7    B1      = 5E-6
+KETA    = -3.304026E-4   A1      = 5.748842E-4    A2      = 0.8367628
+RDSW    = 150            PRWG    = 0.2308827      PRWB    = -0.1982018
+WR      = 1              WINT    = 5.351515E-9    LINT    = 2.047149E-8
+DWG     = 6.185345E-9    DWB     = 1.497881E-8    VOFF    = -0.0821831
+NFACTOR = 2.2623633      CIT     = 0              CDSC    = 2.4E-4
+CDSCD   = 0              CDSCB   = 0              ETA0    = 4.046676E-3
+ETAB    = -8.738959E-4   DSUB    = 6.503103E-3    PCLM    = 0.1698941
+PDIBLC1 = 0.1699085      PDIBLC2 = 0.01           PDIBLCB = -0.1
+DROUT   = 0.718344       PSCBE1  = 6.626429E9     PSCBE2  = 5.004995E-10
+PVAG    = 3.150808E-3    DELTA   = 0.01           RSH     = 6.3
+MOBMOD  = 1              PRT     = 0              UTE     = -1.5
+KT1     = -0.11          KT1L    = 0              KT2     = 0.022
+UA1     = 4.31E-9        UB1     = -7.61E-18      UC1     = -5.6E-11
+AT      = 3.3E4          WL      = 0              WLN     = 1
+WW      = 0              WWN     = 1              WWL     = 0
+LL      = 0              LLN     = 1              LW      = 0
+LWN     = 1              LWL     = 0              CAPMOD  = 2
+XPART   = 0.5            CGDO    = 4.24E-10       CGSO    = 4.24E-10
+CGBO    = 1E-12          CJ      = 8.15989E-4     PB      = 0.8275674
+MJ      = 0.5396637      CJSW    = 1.810068E-10   PBSW    = 0.8
+MJSW    = 0.2976049      CJSWG   = 3.3E-10        PBSWG   = 0.8
```

```
+MJSWG   = 0.2976049      CF      = 0              PVTH0   = -8.567355E-3
+PRDSW   = 1.000265       PK2     = 8.303493E-3    WKETA   = -4.059848E-3
+LKETA   = 7.331573E-3    PU0     = -5.6063179     PUA     = -4.59486E-11
+PUB     = 8.833639E-25   PVSAT   = 264.8251904    PETA0   = 4.288957E-5
+PKETA   = -0.0330423

//  4-Terminal NMOS Model
//  Temperature_parameters=Default

.model pmos1 bsim3v3 type=p
+VERSION = 3.1            TNOM    = 27             TOX     = 4.5E-9
+XJ      = 1E-7           NCH     = 4.1589E17      VTH0    = -0.4202777
+K1      = 0.6047591      K2      = 6.28672E-5     K3      = 0.0894478
+K3B     = 19.8158346     W0      = 1E-6           NLX     = 3.630182E-8
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.6580732      DVT1    = 0.5053159      DVT2    = -0.3
+U0      = 121.4745117    UA      = 1.651983E-9    UB      = 2.065745E-21
+UC      = -1E-10         VSAT    = 1.862502E5     A0      = 0.7274068
+AGS     = 0              B0      = 1.301942E-6    B1      = 5E-6
+KETA    = 0.0239822      A1      = 0.0619585      A2      = 0.4356847
+RDSW    = 803.0213469    PRWG    = -0.1160769     PRWB    = -0.4734383
+WR      = 1              WINT    = 0              LINT    = 2.903067E-8
+DWG     = -2.848501E-8   DWB     = -1.216193E-8   VOFF    = -0.1297937
+NFACTOR = 1.4885005      CIT     = 0              CDSC    = 2.4E-4
+CDSCD   = 0              CDSCB   = 0              ETA0    = 1.131083E-11
+ETAB    = -2.286341E-3   DSUB    = 3.993284E-3    PCLM    = 0.1076345
+PDIBLC1 = 0.0708272      PDIBLC2 = 0.0235091      PDIBLCB = -1E-3
+DROUT   = 0.4412591      PSCBE1  = 1.64623E9      PSCBE2  = 5E-10
+PVAG    = 7.05729E-3     DELTA   = 0.01           RSH     = 6
+MOBMOD  = 1              PRT     = 0              UTE     = -1.5
+KT1     = -0.11          KT1L    = 0              KT2     = 0.022
+UA1     = 4.31E-9        UB1     = -7.61E-18      UC1     = -5.6E-11
+AT      = 3.3E4          WL      = 0              WLN     = 1
+WW      = 0              WWN     = 1              WWL     = 0
+LL      = 0              LLN     = 1              LW      = 0
+LWN     = 1              LWL     = 0              CAPMOD  = 2
+XPART   = 0.5            CGDO    = 4.88E-10       CGSO    = 4.88E-10
+CGBO    = 1E-12          CJ      = 1.165977E-3    PB      = 0.8214639
```

```
+MJ      = 0.4256548      CJSW    = 1.220056E-10   PBSW    = 0.8008
+MJSW    = 0.1001         CJSWG   = 4.22E-10       PBSWG   = 0.8008
+MJSWG   = 0.1001         CF      = 0              PVTH0   = 1.02743E-4
+PRDSW   = -5             PK2     = 9.320893E-5    WKETA   = 0.0307312
+LKETA   = -0.0129391     PU0     = 1.7611588      PUA     = 1.189658E-10
+PUB     = 0              PVSAT   = 50             PETA0   = 1E-4
+PKETA   = -3.992172E-3
```

```
.model pnp1 bjt type=pnp
+ is=2.064e-16 eg=1.169 xti=2.200 nf=1.010
+ ise=94.594f ne=1.740 ikf=90.090m vaf=16 bf=31 xtb=1.280 nr=1
+ isc=7.437f nc=1.500 ikr=39.967m var=3.100 br=15 rc=20.269
+ trc1=2.165m trc2=12.019u re=225.064m tre1=250u tre2=0 rb=7.361
+ trb1=1.141m trb2=6.758u rbm=5.888 irb=57.330m cje=565.109f
+ mje=500m vje=990.003m fc=950m cjc=675.378f mjc=310m vjc=800m
+ xcjc=350m cjs=1.074p mjs=400m vjs=790m tf=16p tr=36n xtf=1
+ vtf=1.200 itf=40.096m ptf=25 kf=6.600e-16 af=1
```