Design of the Analog Front End Circuit for X-Ray Detectors

by

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Declaration

This is to certify that

(i) this thesis comprises my original work towards the degree of Master of Technology in Information and Communication Technology at DA-IICT and has not been submitted elsewhere for a degree,

(ii) due acknowledgement has been made in the text to all other material used.

Signature of Student

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This is to certify that the thesis work entitled *Design of the Analog Front End Circuit for X-Ray Detectors* has been carried out by *Mr. Subhash Chandra Roy (200711020)* for the degree of Master of Technology in Information and Communication Technology at DA-IICT under my supervision.

Thesis Supervisor

(Prof. Chetan Parikh)

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Abstract

The Thesis presents a novel idea to efficiently read out the value corresponding to incident X-Ray, from X-Ray sensor. A system level solution has been proposed which is unique in itself in terms of approach. A simple design of analog front end circuit for 64 channels, consisting of Charge Sensitive Preamplifier (CSP), Pulse Shaping Amplifier (PSA), Peak Detector, Subtractor, Mux and ADC has been proposed. In CSP, Transmission Gate (TG) has been used, in parallel with integrating capacitor, where the NMOS is operating in weak inversion, when TG is supposed to be off. It fulfils the requirements like posing very high ac resistance, providing alternative path for DC leakage current signal, discharging integrating capacitor quickly etc. An amplifier cum level shifter has been used to match the output DC level of CSP with input DC level of PSA. PSA has been implemented as a 4^{th} order Bessel-Butterworth low pass filter, which provides good step response, and hence output is obtained with negligible peaking. High pass filter hasn't been used to avoid low frequency signal loss. A subtractor has been proposed after the peak detector, which is taking care of offset voltages and low frequency noise. This system till the output of shaper is providing a resolution of 1.7% against the specification of 3%.

List of Principal Symbols and Acronyms

k	Boltzmann's constant
π	3.1415926535897932
DC	Direct Current
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
CSP	Charge Sensitive Preamplifier
PSA	Pulse Shaping Amplifier
LSA	Level Shifter cum Amplifier
BW	Band Width
PM	Phase Margin
UGF	Unity Gain Frequency
BB	Bessel-Butterworth
EDB	Equiripple Delay-Butterworth
OTA	Operational Transconductance Amplifier
GBC	Gain Boosted Cascode
Op-Amp	Operational Amplifier
LPF	Low Pass Filter
HPF	High Pass Filter
BPF	Band Pass Filter
TG	Transmission Gate
ADC	Analog to Digital Converter
ROIC	Read-Out Integrated Chip
Q	Quality Factor
Ee	Error Energy
CS	Common Source
CD	Common Drain
CG	Common Gate
CDS	Correlated Double Sampling

CZT	Cadmium Zinc Telluride
SDD	Silicon Drift Detector
PAD	Pixel Array Detector
ASIC	Application Specific Integrated Chip
LCC	Leakage Current Compensation
ppm	parts per million
FFT	Fast Fourier Transform
SPICE	Simulation Program with Integrated Circuit Emphasis
MATLAB	MATrix LABoratory
MCA	Multi-Channel Analyzer
ENC	Equivalent Noise Charge
FWHM	Full Width Half Maximum
r.m.s	root mean square
w.r.t	with respect to
CMRR	Common Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio
ICMR	Input Common Mode Range
SNR	Signal to Noise Ratio
SOI	Silicon On Insulator
SOS	Silicon On Sapphire
PCB	Printed Circuit Board
C1XS	Chandrayaan-1 X-ray Spectrometer
HEX	High Energy X-ray spectrometer
CCII	Second Generation Current Conveyor
S/H	Sample and Hold

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Chapter 1

Introduction

1.1 General

Much research is being done on detection of X-Rays and other radiations like gamma rays etc. Different applications have different constraints, so different approaches use to be taken. Different areas where these detectors are extensively used are: Astro-particle Physics Experiments, Nuclear Reaction Experiments, Chemical Experiments, Medical Applications, X-Ray Spectroscopy, Gamma-ray imaging applications etc.

X-Ray Spectroscopy is having huge and totally diverse applications; some of them are as follows:

1) It is element specific, so, it provides information about a particular element even in complex systems. Hence, it is used in chemistry related experiments.
2) It can be used on solids, liquids, solutions and even gases. It can detect very low concentrations of elements, as low as 10 ppm. So, it is used in chemical analysis.
3) In medical applications, using X-Ray spectroscopy internal structure of any body part is studied and deformities (like tumors, broken bones, ligaments etc), if any, are diagnosed.
4) The rays emitted by elements, while they come back to their normal state from excited state, are similar to its signature i.e. unique to it and hence it is used to characterize composition of any material. Here it will be used to find composition of moon's surface. In Chandrayaan-1, C1XS was used to measure absolute and relative abundances of major rock-forming elements (principally Mg, Al, Si, Ti, Ca and Fe) over the lunar surface [27, 28].
5) Normally the traces of heavy metal (like Uranium) present in any material, decays to lighter metals (like Lead). By finding the concentration of these heavy and light metals, using X-Ray spectroscopy, age of any material can be easily predicted. Here it will be used to predict the age of moon. In Chandrayaan-1, HEX was used to study low-energy (30–270 KeV) gamma rays emitted from the lunar surface due to decay of Uranium and Thorium [26, 29].

Just detection is not enough, the design of readout circuit (part of front end) is equally crucial. All the readout circuits essentially contain a preamplifier and a shaping filter.

There are some core issues which have to be taken care of, for making a good detector and readout circuit.

1) Overall system noise should be very low
2) Power dissipation should be low to avoid thermal effects
3) Dynamic range of the system should be very large, which will ensure high SNR

The following research proposes an approach which will satisfy all the above mentioned requirements better than existing detector and readout circuits. The results obtained are better than the papers used as reference. The proposal concentrates more on the design of the preamplifier and the shaper, which have been the module contributing to maximum noise and power dissipation. Later sections will explain the details of the proposed scheme.

1.2 Motivation

The project has been proposed by Physical Research Laboratory (PRL), Ahmedabad. They have also provided realistic specifications for the ASIC. It is anticipated that, when completed, this design will be used for X-ray detection experiments in ISRO's second moon mission (Chandrayaan-II). It is anticipated that this design will be used for X-ray Spectroscopy in ISRO's second moon mission (Chandrayaan-II). In the first moon mission (Chandrayaan-I), C1XS and HEX payloads were used for similar purpose but for different X-Ray Range [26-29].

1.3 Organisation of the Thesis

Chapter 2: This chapter mainly focuses on the literature survey for problem in hand. It also explains the function of some of the main design blocks used in a typical readout chip.

Chapter 3: This chapter mainly discusses the system level requirements/constraints and specifications for the design. It also shows some of the Mathematical calculations required for deriving specifications of some of the design blocks.

Chapter 4: In this chapter my own idea regarding the overall circuit has been proposed. Also the methodology followed to design the same has been discussed.

Chapter 5: The simulation waveforms and results have been covered in this chapter. The actual results have been compared with theoretical/expected results.

Chapter 6: Here conclusions, future work and some of the miscellaneous but important issues have been discussed in length.

Chapter 2

Background

2.1 Literature Survey

Radiation Sensors and corresponding readout circuits are available in a variety of configurations. They are well-known circuit blocks because of their wide spread applications and hence, basics of their operation can be found in various texts, or on the web. In a conventional detector setup, a sensor module, a preamplifier, shaping filter, peak detector and ADC are used. Some applications need multi-channel detectors which need multi-channel readout circuits. Such circuits have additional blocks like peak stretcher, discriminator, addressing unit, comparator, multiplexer and output buffers [6]. In some ASICs, apart from these blocks some other blocks like, Overload Recovery circuit, Leakage Current Compensation circuit, Baseline Restorer circuit, Ballistic Deficit Correction circuit etc are also included, to take care of abnormal conditions.

Different components of the detector setup have been studied as a part of literature survey. Let us discuss about detector module. The detectors are either (i) intrinsic semiconductor based or (ii) Reverse biased p-n junction based. Some of the detector modules studied is: microstrip detector [9], CdTe detector [11], CZT detector [10, 12], Schottky junction based SiC pixel detector [1], Silicon Drift Detector (SDD) [13, 14, 15, 18] and Pixel Array Detector (PAD) [17]. Pixel pitch and pixel area are important parameters for detector design [10]. These parameters affect detector sensitivity, charge collection time, noise as well as magnitude of leakage current. Typical values for dimensions of the detector pixels are between 100 and 400 microns on a side [1, 17].

Most of the papers emphasize the preamplifier design, as it is reported to be a major contributor to noise and power dissipation [1]. Generally, more than 90% of the noise of the readout electronics is given by the charge preamplifier, so that particular care in the design of this stage is required [1]. Different papers suggest different designs for the preamplifier. The thumb rule is to minimize the number of transistors (especially terminal transistors) in the preamplifier design while meeting other specifications [1].

In some applications, preamplifier circuit has used a pole-zero networks in series with them. The pole-zero (PZ) circuit is an exact replica of the feedback circuit used for the amplifier and forms a self compensating pole-zero networks [6]. The reason behind using the replica circuit is: it cancels the pole introduced by CSP feedback circuit, which leads

to undershoot in the output. This module is optional if CSP and shaper are being separated by some buffer or amplifier.

To reduce the effect of increase in leakage current, as a result of damage caused to the detector by radiation, a leakage current compensation (LCC) unit has been used in parallel with the preamplifier in some designs [3, 106].

Overload Recovery circuits are used taking care of situations when sudden charge pulses with very high energy (outside the expected range) appears. These circuits reset the system and makes sure that the system recovers from such events in very less time.

A variety of options are available for implementation of the shaping filters. Some of the major configurations studied are: semi-Gaussian shaping filter [1, 92], cascading of RC integrator cells [6, 92], switched gain shaper [3], Trapezoidal Shaper (time-variant [88, 92, 95] & time-invariant [90-92]), Quasi-Trapezoidal Shaper [93], Quasi-Triangular Shaper [89, 92], Sin^n x shaper [87], Rectangular Shaper with delay line [94], Suitable number of stages of low pass filter and some other ad hoc solutions [86, 88, 96-98].

2.2 Basic Building Blocks

The following figure shows the most important blocks in any readout circuit:

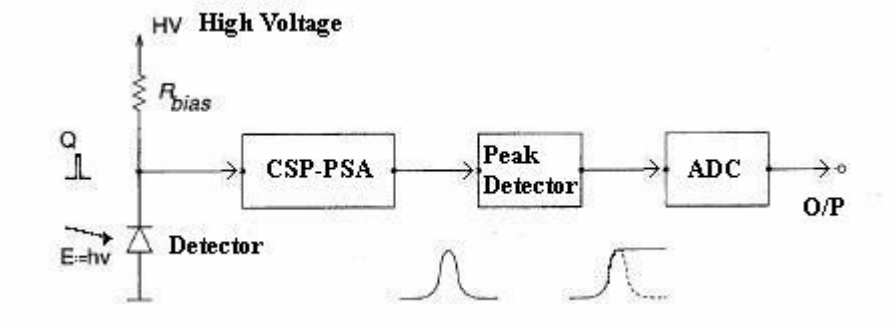

Fig 2.1: Important blocks of a readout circuit

The most basic and important blocks of the design for which special care should be taken are [1, 71]:

Charge Sensitive Preamplifier (CSP) and Pulse Shaping Amplifier (PSA).

These blocks have been discussed in length in the following section.

2.2.1 Charge Sensitive Preamplifier

The task of this block is to simply integrate the input current signal. Lower the value of integrating capacitor, higher will be current to voltage conversion factor .i.e. higher sensitivity of CSP [8, 20, 31-33, 37, 41-45, 50, 113]. The integration task can be essentially done by simple capacitor connected in parallel with the incoming signal. The value of desired components should always be much higher than the parasitic components. As the detector parasitic capacitance is in pf range, the value of integrating capacitor required should be in tens of pf. Clearly, with such a high value of integrating capacitor, sensitivity of CSP will be very low. To solve the contradicting problems of sensitivity and parasitic capacitance, miller effect is used. So, the current CSP looks like this:

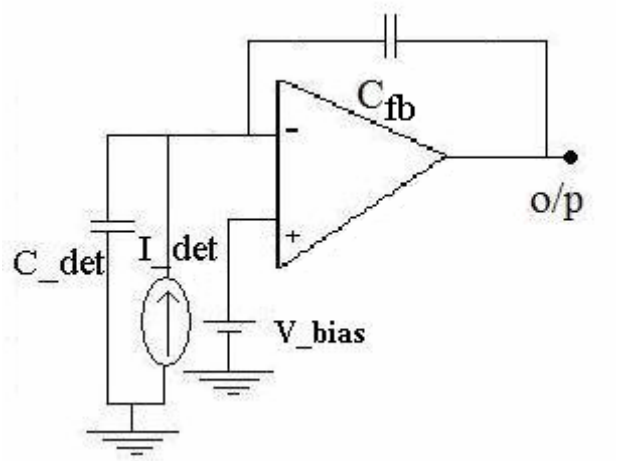

Fig 2.2: Basic structure of CSP

It consists of an inverting amplifier (with voltage gain –A) and a feedback capacitor C_{fb} connected from the output to the input. As the amplifier have infinite input impedance, no current flows into the amplifier input.

If an input signal produces a voltage v_i at the amplifier input, the voltage at the amplifier output is $A*v_i$.

Thus, the voltage difference across the feedback capacitor $v_f = (A+1)*v_i$ and the charge deposited on C_{fb} is $Q_f = C_{fb}* v_f = C_{fb}(A+1)v_i$. Since no current can flow into the amplifier, all of the signal current must charge up the feedback capacitance, so $Q_f = Q_i$. The amplifier input appears as a "dynamic" input capacitance [19, 20, 34]:

$C_i = Q_i/v_i = C_{fb}(A+1)$

The voltage output per unit input charge [20]

$A_Q = dv_o/dQ_i = Av_i/C_iv_i = A/C_i = A/(A+1) * 1/C_{fb} = 1/C_{fb}$ $(A >> 1)$

So, the charge gain is determined by a well-controlled component, the feedback capacitor. The signal charge Q_S will be distributed between the sensor capacitance C_{det} and the dynamic input capacitance C_i.

The ratio of measured charge to signal charge [20]

$Q_i/Q_S = Q_i / (Q_{det} + Q_i) = C_i / (C_{det} + C_i) = 1 / (1 + C_{det}/C_i)$

So, to prevent signal loss at the input of preamp, the dynamic input capacitance must be large compared to the sensor capacitance.

Charge-to-voltage gain of the charge sensitive preamplifier is inversely related to the feedback capacitance.

Charge-to-voltage gain $\approx 1/C_{fb}$

To get the biggest gain we should decrease the feedback capacitance. However, its value must be larger than the parasitic capacitance value divided by the open loop gain factor as follows:

$C_{fb} >> C_{parasitic}/A$

Where, $C_{parasitic} = C_{det} + C_{in\_preamp}$

The underlying op-amp used for CSP should be linear in nature else it will introduce non-linear noise and harmonic distortion [48].

2.2.2 Pulse Shaping Amplifier

Pulse shaping amplifier is also referred to as shaper. A trivial and often neglected function of the shaping amplifier is to amplify signals [99]. The more sophisticated function of a shaping amplifier is to shape the signals to optimize spectrometer performance. It is effectively a filter which removes some of the frequency components from the input signal depending on the cut-off frequency chosen, so shape of output pulse changes slightly, hence it got its name as shaper.

Regarding its function; it restricts the bandwidth, as too large a bandwidth will increase the noise without increasing the signal (outside the signal bandwidth) [38]. Typically, the pulse shaper transforms a narrow sensor pulse into a broader pulse with a gradually rounded maximum at the peaking time, so that peak value can be easily measured [20].

Removal of frequency components results in broadening of the output pulse, so output pulse width increases. The design need to constrain the pulse width so that successive signal pulses can be measured without high probability of overlap (pileup). Also, reducing the pulse duration increases the allowable signal rate.

A high-pass filter sets the duration of the pulse by introducing decay time constant T_d. Next a low-pass filter increases the rise time to limit the noise bandwidth. The high-pass is often referred to as a "differentiator", since for short pulses it forms the derivative. Correspondingly, the low-pass is called an "integrator". Since the high-pass filter is implemented with a CR section and the low-pass with an RC, this shaper is referred to as a CR-RC shaper. In general, more sophisticated and complicated, CR-$(RC)^n$ shapers are used to achieve the desired results [1, 20, 92].

The name of the shaper (like Gaussian, triangular, trapezoidal etc) is given based on the shape of output pulse when a step input is applied.

As per literatures survey, accompanied by mathematical proofs, if the output pulse is having smaller flat region then parallel current noise component will be less, whereas if the output pulse is having slant region with smaller slope then series voltage noise component will be less [74].

Going by the above philosophy, it has been found mathematically that Cusp shape is having minimum output noise, followed by Gaussian [39, 92], Triangular, Quasi-Triangular, Quasi-Trapezoidal [93] (Time Variant and Time Invariant versions), Semi-Gaussian [1, 92], Sin^n x [87, 92], Trapezoidal etc [90-95]. Unfortunately, Cusp [92], Gaussian [92] and Triangular [92] shapers are not practically realizable, because they are non-causal in nature.

All of the above mentioned shapers are mainly a combination of HPF and series of LPF with the output of each stage weighted properly and summed up at the output [90].

In literature at most of the places, an approximation of Semi-Gaussian or Trapezoidal shapers has been used. A Semi-Gaussian Pulse Shaper gives good SNR values. But an ideal Semi-Gaussian filter is non-causal and hence not physically realizable, so it is approximated by using CR-$(RC)^n$ filters [1, 92].

Chapter 3

System Overview

3.1 Brief summary of the actual system

The complete X-Ray detector sensor will be made up of pure intrinsic Silicon, having 64 pixels arranged as an array of 8 x 8 pixels. There will be an independent readout channel corresponding to each pixel. So, there will be 64 readout channels on the ASIC. Hence, all the ASIC components for a channel have to be accommodated in the pixel area.

Each detector pixel will be having dimensions of 2mm x 2mm. So, readout circuit corresponding to a pixel/channel has to be accommodated within an area of $4mm^2$. The thickness of the sensor will be approx 0.5 mm. So, detector capacitance (C_{det}) is:

C_{det} = (permittivity of silicon) * (area of sensor) / (width of sensor)

$= (11.8 * 8.854 * 10^{12}) * (4 * 10^{-6}) / (5 * 10^{-4})$

= 840 ff (approx. 0.85pf)

3.2 Approach

The thesis goal is to develop a low noise; low power and high dynamic range front end read out circuit for X-Ray Sensors.

First the design will be made for single channel detector and optimised, and then it will be replicated for multiple channels, with the addition of a few new blocks, like analog mux, addressing unit etc. As the sensor will be having 64 pixels arranged as a matrix of 8 x 8, there is requirement of independent readout circuits for each of the 64 channels.

The ROIC will be dc coupled to the sensor, because of the following advantages over ac coupling [99]:

1) It minimizes stray capacitances, thereby improving SNR.
2) Higher counting rate is possible.
3) Preamplifier or some other intermediate output can be monitored to measure the leakage current of the detector.

Incoming radiations which are supposed to impinge the X-Ray sensors can cause some damage to ROIC as well, if it is exposed to the rays. So, some of the manufactured chips had used SOI and SOS technologies for fabrication. The current chip is expected to be mounted exactly behind the X-Ray sensor with an intervening PCB. So, it will serve dual

purpose of, (i) tightly coupling sensor to ROIC (i.e. lesser stray capacitance as well as noise) and (ii) protecting the ASIC from incident radiations.
So, normal Si will be sufficient as fabrication material.

3.2.1 Aim of the Design

The aim of the design is to measure the dc value of the integrated current, so, HPF has been avoided. LPF is being used to remove out of band high frequency noise, by providing them very high attenuation in less time.

3.2.2 Capacitance Matching Consideration

The summation of detector capacitance and feedback capacitance should be close to input stage capacitance for keeping the noise low [74, 75]. Mismatch between these capacitors enhances noise by a factor:

$$\left(\sqrt{\frac{C_{in}}{C_{det}+C_{fb}}}+\sqrt{\frac{C_{det}+C_{fb}}{C_{in}}}\right)^2$$

So, higher the mismatch higher will be effect of noise. For the simulated system,

C_{in} = 0.8pF, C_{det} = 0.85pf and C_{fb} = 0.05pf.

$C_{det} + C_{fb}$ = 0.9pf

Hence, the capacitances in denominator and numerator are almost matched.

3.2.3 CSP Noise Consideration

Generally, up to 1 MHz 1/f noise is the dominant source noise in the circuits [1]. PMOS have lesser 1/f noise compared to NMOS. So, PMOS devices have been as input device in all the amplifiers. Two stage amplifiers used in the above circuits give better noise performance compared to its other counterparts.
Noise from the second stage is divided by the gain of the first stage when referred to the main input (Frii's law). Hence, the gain of the preamplifier has been kept very high, so that effect of noise from subsequent stages is negligible.
In MOSFETs, normally thermal noise and 1/f noise are the main source of noises, which are modeled as series voltage noise sources. Shot Noise is modeled as parallel current noise source, is negligible in MOSFET circuits.

Relationship between various important op-amp performance metrics such as speed, SNR and power consumption can be shown as [107]:

$$\frac{\text{SNR} \cdot \text{Speed}}{\text{Power}} \propto \frac{(\text{Swing})^2}{V_{sup}}$$

The proportionality constant is a function of the architecture of the op-amp and feed back circuit.

It is evident from the above equation that, a higher output voltage swing will give better SNR or else speed and power performances can also be improved. So, the underlying op-amp used for CSP has been designed for high output swing and hence the choice of two-staged op-amp architecture is justified.

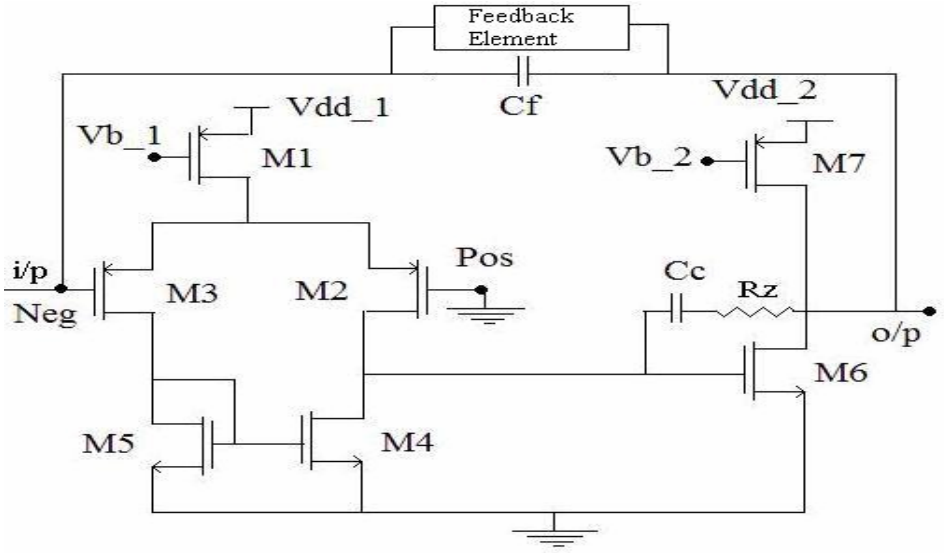

Fig 3.1: Two-Staged Amplifier used for CSP

Input referred noise of the above amplifier is:

$$V_{n,in}^2 = 8kT\left(\frac{2}{3g_{m2}} + \frac{2\,g_{m4}}{3g_{m2}^2}\right) + \frac{2K_N}{C_{ox}(WL)_4 f}\frac{g_{m4}^2}{g_{m2}^2} + \frac{2K_P}{C_{ox}(WL)_2 f}$$

The above noise equation is consisting of thermal noise (1st term) and flicker noise (2nd and 3rd terms), where K_N and K_P are flicker noise coefficients for NMOS and PMOS transistors. At low frequencies flicker noise will be the dominant source of noise for the above amplifier, because it is comprised of MOSFETs.

It is evident from the above equation that, to minimize the flicker noise of source transistors its dimensions should be large i.e. W_{src} and L_{src} should be large. While to

minimize the flicker noise of load transistors its dimensions should be large i.e. W_{load} and L_{load} should be large, but at the same time transconductance of source transistors should be high i.e. W_{src} should be large and L_{src} should be small.

So, we have contradictory constraints on L_{src} value. To find the optimum value of L_{src}, flicker noise equation is differentiated wrt L_{src} and equated to zero. This gives the optimum source transistor length as [84]:

$$L_{src(opt)} = \frac{L_{load}}{\sqrt{\frac{K_{load}\mu_{load}}{K_{src}\mu_{src}}}}$$

This relation has been taken care in the design of above Two-Staged Amplifier, thus ensuring low intrinsic noise contribution.

g_m/I_D Based Methodology [72] was also referred while designing which helps in designing for better transconductance efficiency. It also helps in choosing better tradeoffs between different OTA parameters.

3.3 Calculations

3.3.1 Input current pulse amplitude

As per specs, the read out circuit is supposed to measure energy of X-Rays in the range 3-30KeV. The calculations corresponding to 30KeV X-Rays has been shown.

Number of electrons-hole pair generated will be:

N = (Total incident energy) / (energy gap of silicon)

=30KeV/1.1eV = 27,273

So, total charge generated, $Q = 27{,}273 * 1.602 * 10^{-19} = 4.37 * 10^{-15}$

Once the X-Ray hits the sensor, all the charge is not generated at once, it is generated over a finite time called charge collection time (T_{ch}). For large sensor pixels T_{ch} is quite large and may cause Ballistic Deficit (reduction in output amplitude), if proper care is not taken. For the detector used value of T_{ch} lies in the range of 100ns to 200ns.

Taking, T_{ch} = 100ns,

Value of current peak = $Q / T_{ch} = (4.37 * 10^{-15}) / (100 * 10^{-9}) = 43.7$ nA

3.3.2 Essential BW for incoming signal & integrated signal

As the incoming signal pulse was random in nature, its energy is mainly concentrated at low frequencies. The frequency spectrum of a random signal extends up to infinity, but the energy content of the high frequency components decreases gradually. So, after some particular frequency the energy content of all the higher frequency components can be neglected. This particular frequency is normally referred to as "Essential bandwidth". Essential bandwidth of the incoming signal was calculated by taking its FFT in MATLAB. The limit for essential bandwidth was kept as frequencies which encompass 99% of the total energy [53].

For finding the frequency spectrum of input signal, a test signal with Gaussian shape and 100ns width was taken. FFT was applied on this signal using MATLAB and its amplitude spectrum was noted. The results obtained are as follows:

Total energy of all the frequency components of the signal (Eg) = 15, 50,024

(Note: Energy is proportional to amplitude*amplitude i.e. amplitude^2.)

Error Energy (Ee) = 1% of Eg = 15,500.24

Summation of all the frequency components above 6,498 constitutes a value almost equal to Ee. So, significant frequency range = 6,498 * 1 KHz = 6.498 MHz (approx 6.5 MHz)

So, using R_{fb} is not appropriate as it causes low frequency signal loss.

Following the above method and keeping Ee = 1%, 0.5% & 0.1%, the essential bandwidth for the integrated signal were calculated, which comes out to be 100 KHz, 300 KHz and 980 KHz respectively.

3.4 Specifications

The specifications for the ASIC are as follows:

Expected Count Rate	1000 Pulses/second/cm^2
Rise Time	100 ns
Pulse Width	100 to 200 ns
Shaping Time	0.5 to 2 μs
Detector Range	Range 3 – 30 KeV (optimum at 6KeV)
Resolution	3% resolution (200eV @ 6KeV)
Temperature Range	-12 to 20 Degrees Celsius

Voltage Across Wafer	30 to 40 V
Total number of channels	8 x 8 channel pixel detector
Power Dissipation per channel	< 0.5mW
Max. allowed Noise Charge	200 electrons r.m.s

Table 3.1: Specifications for the ASIC

Maximum allowed ENC at input = 200 electrons r.m.s

$= 200/0.707 = 283$ electrons

$= 283 * 1.602 * 10^{-19} = 453.4 * 10^{-19}$ C

As minimum signal pulse width is = 100 ns = 10^{-7} s

So, max. allowed noise current at the input = $4.534 * 10^{-17} / 10^{-7}$

$= 4.534 * 10^{-10}$ A

Other relevant details are:

Technology = 0.8u, V_{DD} = 3.3V, C_{load} = 0.1pF, Feedback Capacitor (C_{fb}) = 50fF

As maximum power dissipation per channel is 0.5mW. The power has been distributed among different blocks as follows:

P_{d_preamp} = 0.1mW/Channel

$P_{d\_digital\_logic}$ = 0.05mW/Channel

P_{d_shaper} = 0.25mW/Channel

P_{d_ADC} = 0.1mW/Channel

A CSP with nearly similar specifications has recently been published in IET Circuits Magazine [113].

3.5 Design and Analysis

The aim is to accurately measure the energy of the incident x-ray. The sensor will give a sharp charge pulse as output proportional to the incident energy. As measuring the charge is not convenient, so it is converted into a voltage pulse via a Charge Sensitive Preamplifier (CSP). Hence, the amplitude of output voltage pulse is proportional to the energy of the incident x-ray. Thus, making sure all the charge gets transferred to the preamplifier is a critical issue. CSP being the first stage of the readout chip, its open loop gain should be very high and its intrinsic noise should be very low.

The main design objective is to reduce total noise in the final output. We know output noise is directly proportional to the bandwidth of the system. So, it is desirable to have as low bandwidth as possible. One should keep the system bandwidth only as much as dictated by the signal bandwidth. Hence, knowing the frequency spectrum of the input charge pulse is important.

All the blocks in the design, will be designed so as to make sure that the intrinsic noise contribution of each block is minimum, for which following rule of thumb will be followed:

"The transconductance must be maximized if the transistor is to amplify a voltage signal applied to its gate, whereas it must be minimized if the transistor operates as a current source" [19].

Pulse Shaping Amplifier (PSA) is not supposed to impart very high gain, but they are supposed to shape the input pulse so as to reduce its noise content. At the most basic level pulse shapers can be thought of as band pass or low pass filters depending on nature of input, having desired lower and upper cut-off frequencies. They also transform a narrow sensor pulse into a broader pulse with a gradually rounded maximum at the peaking time.

Chapter 4

Proposal

4.1 Proposed Solution

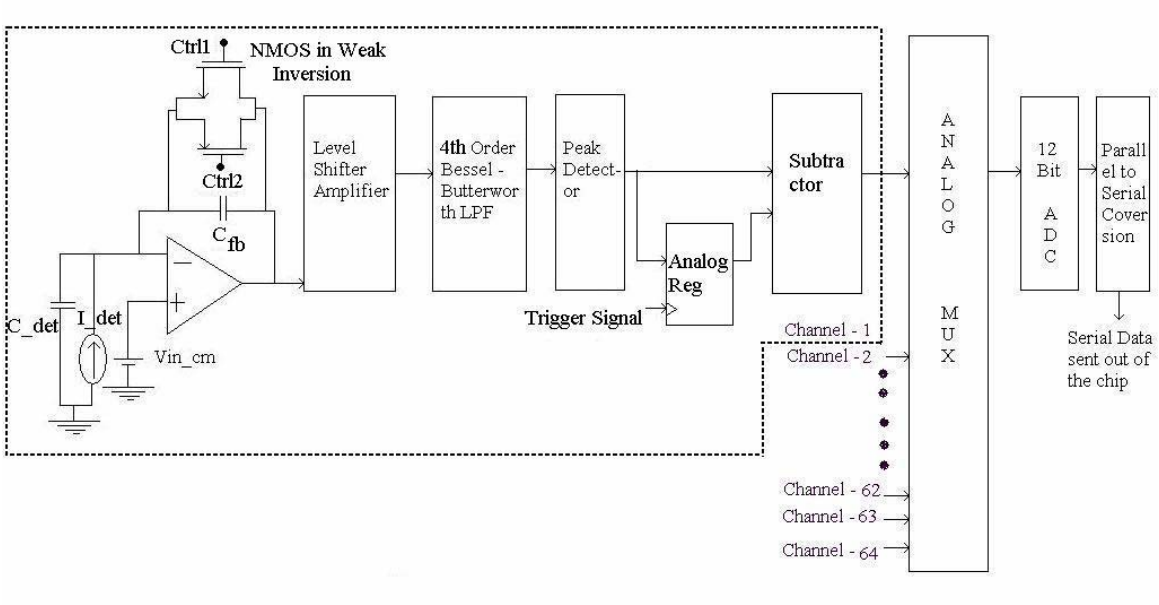

Fig 4.1: Proposed overall block diagram

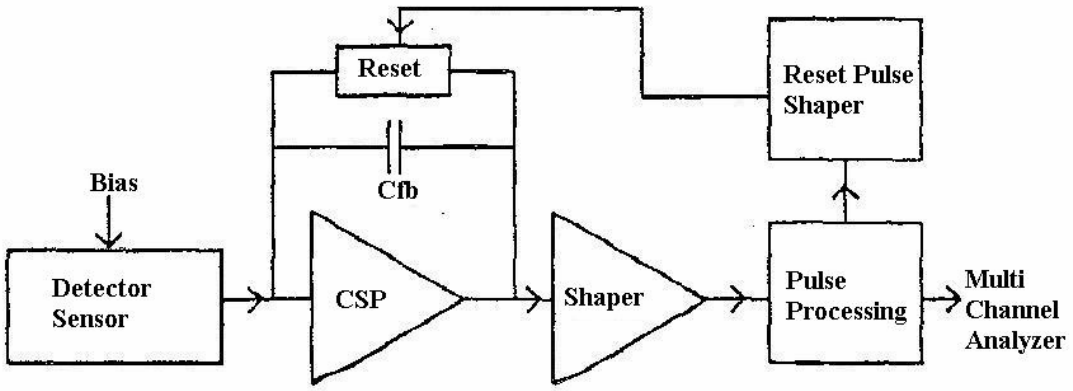

Fig 4.2: Analog Channel showing source of reset pulse [69]

4.1.1 Explanation

The X-Ray sensor generates output current pulse when any X-Ray hits it, in the rest of the time detector will generate some small DC leakage current. Almost all the signal current will flow through the integrating capacitor connected in feedback (C_{fb}) while the leakage current will flow through the transmission gate connected in parallel with C_{fb}. Output voltage of CSP goes to the amplifier which amplifies it by a factor of 15. The

intermediate amplifier stage is designed to serve dual purpose, of amplifying the weak voltage signal as well as providing level shifting to match output DC level of CSP with input DC level of shaper. Output of amplifier then goes to Shaper, which is mainly 2 staged, 4^{th} order Bessel-Butterworth Filter, which as a whole gives a gain of 0.9. These active filters use op-amp as their basic building block and the op-amps are typically emulated using Operational Transconductance Amplifier (OTA) followed by very low output buffer stage. Here OTA instead of op-amps has been used as the basic building block for the filter. To handle the problem of high output impedance of OTA, they have been used in unity gain feedback mode. Thus both area and power consumed by the required output buffers, for an op-amp, has been saved. The output of Shaper will go to the peak detector, as the peak value of final output voltage will be directly related with the energy of incident X-Ray. When the integrating capacitor (C_{fb}) is discharged i.e. the system is in reset phase, output of peak detector will be stored in an analog register (Sample and Hold Circuit). Output at this time will be due to input DC offset voltage and noise (mainly 1/f noise). This stored peak value will be subtracted from the output of peak detector, when peak value corresponding to valid signal is there. As the low frequency noise value doesn't change much during this period of time, the subtraction operation will effectively, remove DC offset and low frequency noise and hence signal to noise ratio (SNR) will improve significantly.

When this architecture will be extended to multiple channels, an analog multiplexer have to be used to choose one of the channels and send its analog output voltage to a common 12 bit Analog-to-Digital Converter (ADC). A parallel to serial converter unit will convert 12 bit parallel output into serial form and the resulting bit stream will be sent out of the chip serially.

4.2 Implementation of Charge Sensitive Preamplifier

As CSP is the first as well as most critical stage of the whole ASIC it was designed first. The important issue was to decide the right type of base OTA for CSP. All the well known OTA configurations, i.e. Telescopic Cascode [19, 23, 107]; Folded Cascode [19, 23, 84]; Two Stage [19, 23, 84] and Gain Boosted Cascode [19, 23, 100] were explored for their merits and demerits to choose the most suitable topology.

Telescopic Cascode topology was the far better than other topologies in terms of gain, frequency response, noise and speed but it was not suitable for use in unity gain feedback

mode due to limited output voltage swing. Similar was the problem with Gain Boosted Cascode. Folded Cascode was noisier compared to other topologies due to higher number of terminal transistors. Two-Stage Amplifier was a good choice but it has the problem of stability, due to insufficient phase margin, which means some sort of compensation is required. There are several techniques for frequency compensation. Some of the important techniques are [19, 33]:

1) Miller Compensation
2) Miller Compensation with source follower
3) Phantom Zero
4) Pole Splitting
5) Pole-Zero Cancellation
6) Resistive Broad banding

All these techniques have its own pros and cons.; to achieve better trade-off of PM and UGF one need to go for complex techniques like Phantom Zero [33].

For the current system above problem was solved by using RC (pole-zero cancellation) compensation. Values of the compensating components are:

$C_C = 2pf$ and $R_Z = 40KOhm$

Simulation results with and without compensation:

Parameter	Without Compensation	With Compensation
Gain	81.68 dB	81.68 dB
Band Width	83.6 KHz	887 Hz
Unity Gain Frequency	21.1 MHz	13.5 MHz
Phase Margin	4.2 Degrees	90.4 Degrees
CMRR	66 dB	70 dB
PSRR	58 dB	65 dB
Output Voltage Swing	2.65 V	2.65 V

Table 4.1: Two-Stage Amplifier performance with compensation & without compensation

Higher Phase Margin (PM) gives better results so, comparatively higher PM has been kept. Some papers also suggest to keep PM > 70 Degrees [25, 65].

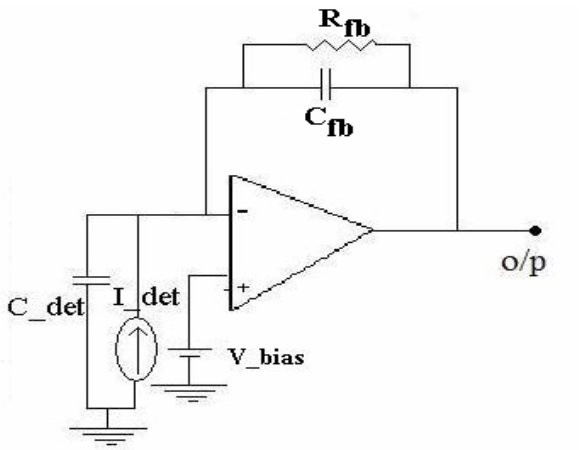

Fig 4.3: Initial CSP setup used for simulations.

4.2.1 Doublet Discussion

When a pole and a zero are spaced closely, they are called doublet. Doublet has bad influence on settling. It can be generated by:

1) Current mirrors used for doing differential to single-ended output conversion.
2) Feed forward capacitor in a voltage follower.
3) In pole-zero cancellation, when pole and zero is not perfectly matched.

The effect of pole-zero doublets could be not clearly seen in the amplitude and phase response, especially in the case, if they are closed together, but relatively small mismatch can have high impact on time response. In time response there will be an overshoot along with slow settling time. So, one may see long settling time in spite of having good PM.

From the fig 4.3, it is visible that, R_{fb}, C_{fb} and C_{det} form a feedback network. It introduces a doublet: a pole and a zero at $1/R_{fb}(C_{fb} + C_{det})$ and $1/R_{fb}C_{fb}$ respectively. Normally they appear at frequencies much less than amplifier unity gain frequency, if they appear beyond unity gain frequency their effect will be negligible.

Lower frequency doublets will give a response which persists for a longer period but with smaller ringing amplitude. Higher frequency doublets will give a response which dies out faster but has larger ringing amplitude [114].

In CSP, if C_{fb} is decreased then the separation between the pole zero doublet increases and the doublet moves towards lower frequency end. As a result its effect on transient response increases and also it causes ringing in the output.

4.2.2 C_{fb} Discussion

Initial simulations were done with C_{fb} = 10ff and R_{fb} = 100MOhm. All the relevant analysis like .ac, .op, .tran and .noise were performed with these values. Transient Analysis showed that output of CSP was ringing for long time before settling down to steady state value, which clearly showed that the system with chosen value of feedback elements was underdamped. One thing worth mentioning here is, normally open loop Phase Margin is kept enough (>=60 degrees) to make sure, the closed loop system is stable. But the implicit assumption is that the feedback network won't introduce any phase shift, which is clearly not the case for the CSP [31-33, 41-44, 86]. The small signal model was drawn for the CSP and corresponding equations were solved. The resulting equations were of 3rd degree. For solving such equations Root Locus can be used. Root Locus tells how the closed loop poles of the system will be moving when different system parameters like open loop gain, feedback factor etc are varied, hence it informs about status of closed loop stability of any system [5, 52]. But, for this design the equations were approximated and were reduced to second order equations of the form:

$$As^2 + Bs + C = 0 \qquad \text{where "s" is Laplace domain variable}$$

In order to avoid ringing in the output one need to make sure that the poles are critically damped or over damped. So, the following condition has to be satisfied:

$$B^2 >= 4 * A * C$$

In terms of actual circuit components this condition becomes:

$$A_0 * S_p * R_{fb} * C_{fb}^2 >= 4 * C_{det}$$

Where, A_0 is DC gain of OTA used for CSP. S_p is the dominant pole of the OTA. It is quite evident from the nature of variables that only R_{fb} and C_{fb} can be varied. So, for satisfying this condition C_{fb} was increased to 50ff as R_{fb} was already very high. Increasing C_{fb} also makes sure the pole zero doublet moves towards higher frequencies.

The output of CSP is being fed to Level Shifter cum Amplifier (LSA). It has been implemented as CS amplifier with resistive load. It mainly shifts the output common mode level of the CSP to match the input common mode requirements for the shaper. The output voltage signal from CSP is having small amplitude, so this module provides necessary voltage amplification as well. In order to make sure that the output signal of Level Shifter cum Amplifier is not getting clipped, the voltage signal from CSP should be within the dynamic range of the Level Shifter cum Amplifier i.e. amplitude of output signal of CSP should be less than ICMR of Level Shifter cum Amplifier.

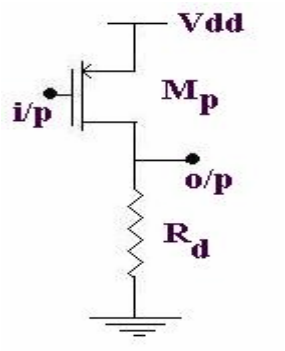

Fig 4.4: Level Shifter cum Amplifier

4.2.3 R_{fb} Discussion

A very high value of R_{fb} is desired so that only the near DC components flow through it and most of the signal components flow through the C_{fb}. Also it's desirable in terms of noise performance. But it increases C_{fb} discharge time. Most importantly, it is very difficult to fabricate such a high value of R_{fb}. Even if it is fabricated, its resistance becomes a function of frequency (very undesirable effect). So, high valued R_{fb} is typically realized as output impedance of high gain OTA.

As the input signal is random in nature and its frequency spectrum is concentrated at low frequencies. Using R_{fb} was causing low frequency signal loss. So, there was a need to look for some other alternative/approach. Whatever circuit is connected in parallel with C_{fb}, it needs to fulfil certain basic requirements.

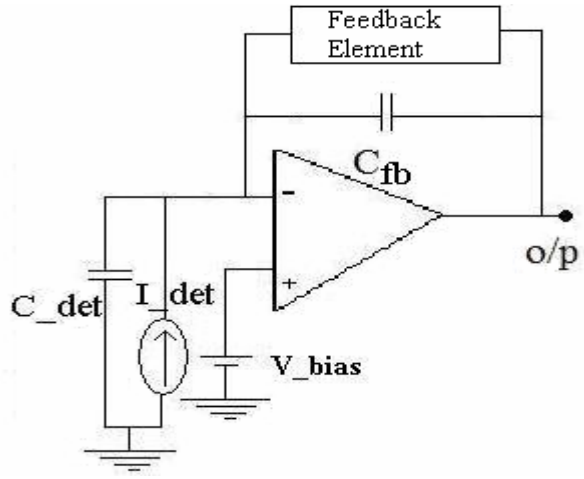

Fig 4.5: Feedback element across C_{fb} required for proper operation of CSP.

4.2.4 Effect of R_{fb} and C_{fb} on Stability of CSP

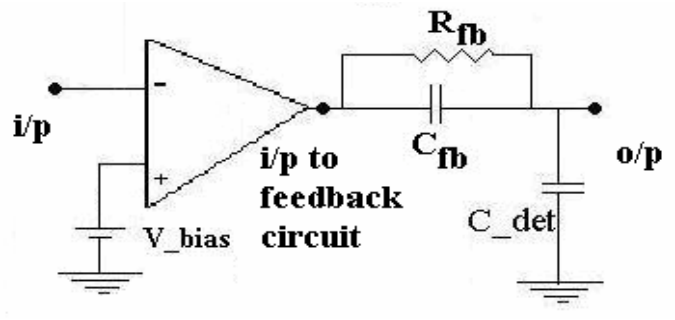

Fig 4.6: CSP Feedback circuit shown separately

With reference to fig 4.3, R_{fb}, C_{fb} and C_{det} form a feedback network. f(s) is the feedback factor.

$f(s) = [R_{fb}C_{fb}s + 1] / [R_{fb}(C_{fb} + C_{det})s + 1]$

At high frequencies this will reduce to:

$f(s) = C_{fb}/(C_{fb} + C_{det})$

Clearly, decreasing C_{fb} will decrease the feedback factor, f(s), which means stability of the CSP will improve.

Towards the lower frequency range, impedance of C_{fb} will be higher compared to R_{fb}, so the feedback factor equation reduces to:

$f(s) = 1 / [1 + R_{fb}C_{det}s]$

Clearly, increasing R_{fb} will decrease the feedback factor, f(s), which means stability of the CSP will improve.

Hence, stability of CSP improves either by increasing R_{fb} or decreasing C_{fb}.

4.3 Role of Feedback element

The component used for feedback in parallel with C_{fb} has to perform following tasks:

1) Discharge C_{fb} quickly, once the voltage pulse has been read by the ADC.
2) Provide path for leakage current.
3) Make sure all the signal current flows through the C_{fb}.
4) Provide DC feedback to maintain DC bias at the input.

4.4 Existing Techniques for low noise

1) Fabricating input JFET (which is part of 1st stage of Readout circuit), on sensor chip itself [4, 15].
2) BiCMOS technology used where input signals are applied to BJTs [22].
3) Chopper method [22, 111]

4) Correlated Double Sampling (CDS) [61, 62, 108-111].
5) Pulsed-light feedback method for discharging C_{fb} (Optical Isolation is problematic) [33].
6) Voltage controlled switch across C_{fb} [44, 105, 113].
7) Output impedance of telescopic cascode or GBC amplifier as R_{fb} [25, 65].
8) Switched Capacitor circuits [19, 22, 51].
9) Input transistors in weak inversion [22, 64, 78].
10) C_{fb} & R_{fb} as feedback elements, but output connection of C_{fb} & R_{fb} is separated by a buffer [25, 65, 77].

4.5 Approaches tried as a part of Thesis

1) Very high valued R_{fb}: Very high valued R_{fb} was used in parallel with C_{fb}. The near DC components flow through it and most of the signal components flow through the C_{fb}. It was very well satisfying most of the requirements of a feedback element (mentioned in section 4.3).

   Issue with the technique: It is very difficult to fabricate very high value of R_{fb}. Even if it is fabricated, its resistance becomes a function of frequency. Most important issue was, amount of low-frequency signal loss due to R_{fb} was not acceptable.
2) Chopper technique: Input signal is switched (chopped) at a very fast rate (the rate is equal to the carrier frequency), which effectively means input signal is being modulated by carrier frequency. As a result the input signal spectrum moves to a high frequency band. The modulated version of input signal is applied to CSP. The output voltage of CSP is again switched at the same rate. It effectively demodulates the actual input signal but modulates the 1/f noise (moves it to high frequencies). A LPF with suitable cutoff frequency will pass the desired to output and will block low frequency noise.

   Issue with the technique: The high frequency clock will cause large power dissipation. At the output side chopper again samples the signal at the same clock rate, as the input side.
3) Chopper at input and Band pass filter at output: The input setup is same, but at the output instead of another chopper a BPF was proposed which would selectively

pass the signal frequencies blocking everything else. Hence, it can effectively reduce 1/f noise as well as thermal noise.

Issue with the technique: As CSP is an integrator and the input chopper shifts the signal frequency band, so improper integration takes place.

4) Switches at input and across C_{fb}: The idea was to keep both the input and feedback switch open till any valid signal appears at the input. The input switch will close when the input signal appears but the feedback switch will close when the processing of the input pulse is over. So, effectively a feed forward control signal is required for the input switch while a feedback control signal is required for the feedback switch. The idea was to reduce noise and effect of leakage current.

   Issue with the technique: Generating the feed forward control signal is very difficult, as it will require delaying the input signal till the control signal closes the input switch.

5) Current amplifier as the first stage followed by integrating capacitor: The idea was to use a high gain current amplifier as the first stage, then integrate the amplified current signal over a integrating capacitor larger than surrounding parasitic capacitors (lesser I to V conversion ratio). Differential voltage amplifier and other blocks will follow it. This idea was proposed to avoid C_{fb} in feedback, which needed some element in parallel with it satisfying the criteria mentioned in section 4.3.

   Issue with the technique: Implementing a high gain current amplifier with CMOS is difficult and complicated [49]. It will consume large amount of chip area as well, which is an important constraint.

6) Unidirectional element Gm (from output to input), across C_{fb}: Normally Unidirectional element Gm is used (in series with compensation capacitor) for controlling closed loop poles and improving phase margin. Similar philosophy was explored here, in an attempt to achieve desired results.

   Issue with the technique: Common Source (CS), Common Drain (CD) and Common Gate (CG) amplifiers are tried as Gm element but none of them are able to satisfy all the requirements mentioned in section 4.3.

7) Connecting NMOS in Gain Boosted Configuration, to increase overall Resistance: As the goal was to achieve very high value of R_{fb}. So, instead of using simple

resistor, 3 NMOS in Gain Boosted Configuration was connected, expecting a very high value of effective resistance.

Issue with the technique: This configuration gives high resistance only when all the transistors are in saturation. It is very difficult to maintain all the 3 transistors in saturation for whole voltage range. Also, it required a high voltage drop across it.

8) C_{fb} & R_{fb} as feedback elements, but output connection of C_{fb} & R_{fb} is separated by a buffer: This topology was used in some papers and they claimed it gives good results.

   Issue with the technique: This architecture was simulated, the results were not good. Its small signal model also didn't show any improvement. Effectively, it didn't work here.

9) TG switches across C_{fb}, with NMOS in sub-threshold: This is finally the technique which works fine and meets all the above mentioned requirements. It has been discussed in length in the next section.

4.6 Proposed Feedback element

Transmission Gate (TG) switch has been used as the feedback element across C_{fb}, where NMOS will be in sub-threshold region and PMOS will be in off region, when the TG switch is supposed to be off.

For Weak Inversion, the charge in the channel is much lower and drift-current decreases, so the channel resistance is very high. However there is a concentration gradient in the channel that causes diffusion current [73].

The noise performance (especially thermal noise) in weak inversion region is better than strong inversion region [64, 78-82].

Details of weak inversion operation can be found in Appendix-III

Due to very high small signal resistance (~ 10^9 to $10^{10}\Omega$) of NMOS in weak inversion, the cutoff frequency of the integrator occurs at very low frequency, near 100 Hz, so most of the signal current flows through C_{fb} and contributing to output.

During weak inversion diffusion current flows through the transistor, so it is able to sink the small steady state DC leakage current in the absence of valid signal pulse and hence it protects C_{fb} from saturation. This system have been checked to be working properly up to

0.5pA of DC currents, while as per specifications, maximum leakage current for the system will be 0.1pA.

When the processing corresponding to input current pulse is over i.e. when peak detector output is sampled by ADC, pulse processing unit will be generating a trigger signal which will close the TG switch. In ON state both PMOS & NMOS transistors will be having very low resistance, so, C_{fb} will be discharged in very less time and hence very high counting rates can be achieved.

While the TG switch is ON, the underlying Op-amp works in unity gain mode. So, the DC bias at non-inverting input will appear at output, which in turn will appear at inverting input. This DC bias will be stored across the capacitors at each of these nodes. So, same DC bias will be appearing at both inverting and non-inverting inputs. As a result the inverting input node will act as a virtual ground. Whenever signal pulse comes, it passes through inverting input to the output via the feedback circuit and raises the output node potential while input node potential remains almost constant.

So, it is clearly visible that the proposed NMOS in weak inversion is able to satisfy all the requirements mentioned above. Apart from this, it contributes very less noise [78-81] and occupies very less area when compared with R_{fb}.

4.7 Charge Injection and Clock Feedthrough

Charge Injection takes place whenever a MOS switch goes from ON to OFF state. Charge injection is a very complicated effect, because it depends on the input signal. Normally this effect is assumed to be first order effect and hence corresponding solutions have been proposed, like differential sampling technique etc. But its dependence on the input signal makes it a higher order, which can't be removed totally by differential techniques.

It has been mentioned in literature that, if the clock signal turns off fast, the channel charge distributes fairly equally between the adjacent nodes [30, 64, 101-104].

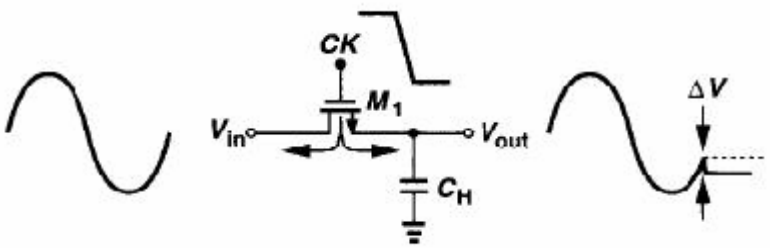

Fig 4.7: Charge Injection shown with NMOS switch [30]

So, total change in voltage across C_{load} is:

$$\Delta v_{load} = -\frac{C'_{ox} \cdot W \cdot L \cdot (V_{GS} - V_{THN})}{2C_{load}}$$

This can be written as:

$$\Delta v_{load} = -\frac{C'_{ox} \cdot W \cdot L \cdot (VDD - v_{in} - V_{THN})}{2C_{load}}$$

The threshold voltage expression can be substituted into the above equation to get:

$$\Delta v_{load} = -\frac{C'_{ox} \cdot W \cdot L \cdot (V_{DD} - v_{in} - [V_{THN0} + \gamma(\sqrt{|2\phi_F| + v_{in} - V_{SS}} - \sqrt{|2\phi_F|})])}{2C_{load}}$$

The change in voltage across C_{load} is non-linear with respect to V_{in} due to threshold voltage. So, charge injection is signal dependant; hence it will cause harmonic distortion. This will result in higher order non-linear errors [30, 101-104].

Apart from charge injection, clock feed through effect will also change the potential across $C_{load.}$ Clock feed through effect comes into picture because clock signal is coupled to the output signal node via Gate-Diffusion overlap capacitance.

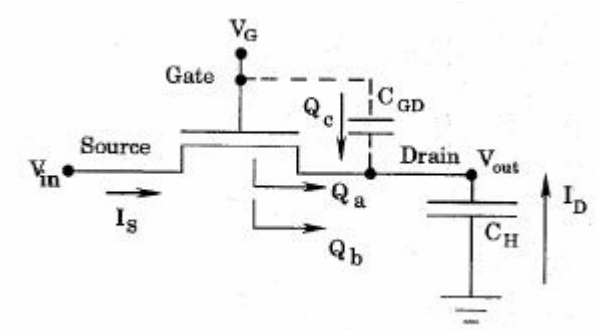

Fig 4.8: Charge Injection (Signal Dependant Qa; Signal Independent Qb) & Clock Feed through Qc [103]

The total unwanted voltage across C_{load} has a signal dependant voltage component and a signal independent voltage component. Canceling the total unwanted voltage (signal dependant + signal independent voltage) is a tough job. It needs very sophisticated switching. One of the techniques proposed in some papers, which claims to remove both signal dependant and signal independent voltage components, is shown below [104].

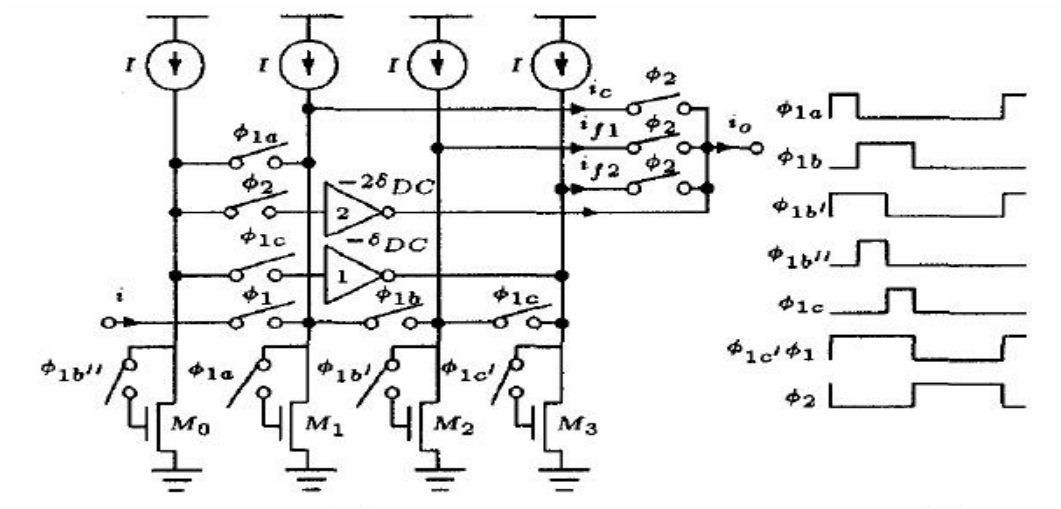

Fig 4.9: Circuit schematic for total charge cancellation (waveform controlling the switches are shown on right side) [104].

The wave form showing effect of channel charge injection on output voltage is shown in the next figure. There is a rise in output voltage level as soon as the clock controlling the NMOS goes from HIGH to LOW i.e. when NMOS gets turned OFF.

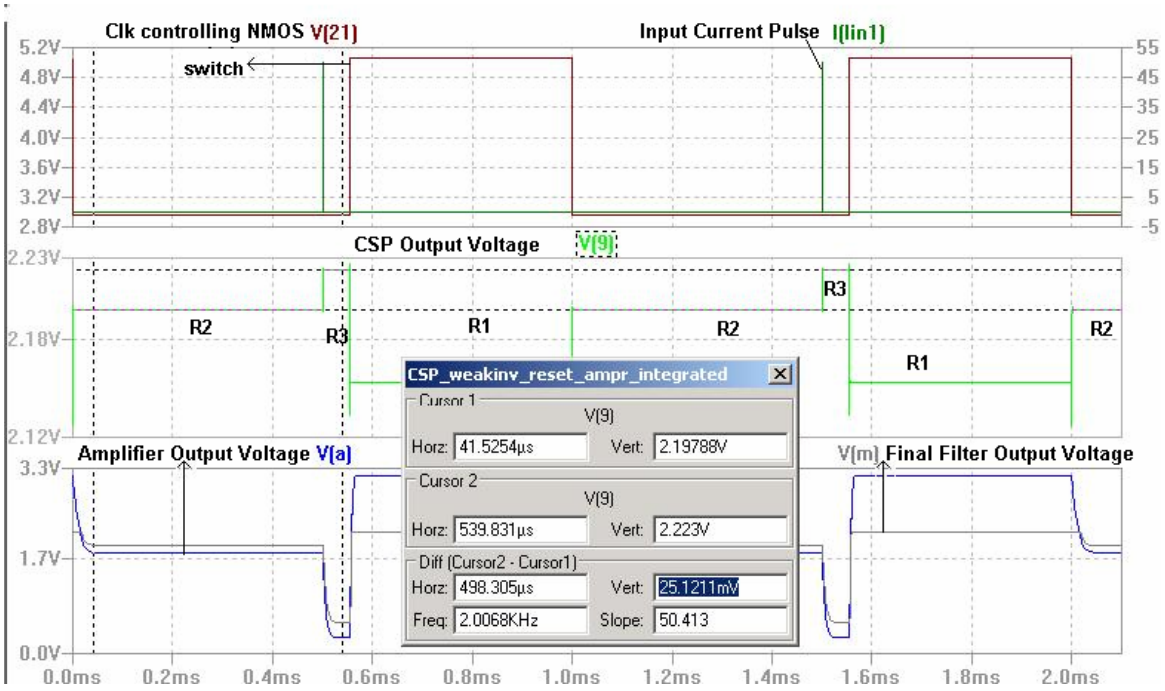

Fig 4.10: Charge Injection effect in output

The philosophy was to keep the things simple. So, simple CMOS switch (TG) has been used, which reduces the voltage amplitude due to charge injection & clock feed through but doesn't cancel the effect totally. As a result, some net charge is injected, which generates some net voltage which can be seen as region R2 in the above waveform.

Region R1 is the voltage level when system gets reset i.e. no voltage over C_{fb}. As soon as the clock goes low and switch opens, some net voltage appears at the output of CSP. This voltage remains constant until current pulse appears from the X-Ray detector sensor, which again charges C_{fb} and output voltage increases. This situation is depicted in the region R3. Region R3 holds its value, till the pulse processing is complete and output level falls to region R1 again.

If the system is not stable or there is some other problem, voltage level corresponding R2 will not remain constant, but it will keep on increasing with time at a constant rate. So, special care has been taken to avoid such condition.

The approach taken here is: "If you can't fight them, join them". So, to tackle the effect of unwanted voltage, double sampling is done. The output voltage will be once sampled when the switch goes ON to OFF and there is no input signal. This value will be stored in some analog register. So, the output at this time will be corresponding to injected voltage (Region R1). The output will be sampled again, after the occurrence of input current pulse (Region R2). Voltage corresponding to region R2 will be subtracted from stored value (i.e. voltage corresponding to region R1). The net result will be corresponding to input signal and free from all the injected voltages.

There are different parameters in SPICE which take care of simulated result of channel charge injection. Some of these are: XPART, CKAPPA, CGS0, CGS1, CGD0, CGD1, and CGB0 [54-57].

XPART decides distribution of total channel charge between drain and source end. For simplicity this parameter is assumed to be 0.5 i.e. total charge distributes equally between source and drain. But the phenomenon of distribution of charge is fairly complicated because the conditions at source and drain end are not same.

Yang, Epler and Chaterjee [54] proposed a value 1 for this parameter i.e. all the charge goes to source region. Their proposal was based on the physical argument that, in saturation the drain is electrically disconnected from the inversion layer.

Ward and Dutton showed number of mathematical calculations and reached at a conclusion that 0.4 is the optimum value for this parameter .i.e. 40% charge goes towards drain end and 60% charge goes towards source end.

Different values for XPART was tried, simulation results didn't showed much variation in the amplitude of charge injected voltage in the output. So, finally XPART = 0.4 was chosen.

The distribution of charge also depends on ratio of capacitance seen at source and drain ends. At source end the capacitance will be mainly Cgs and at drain end it will be Cds. At any end the total capacitance is modeled to have 3 components:

1) Physical overlap capacitance between gate and diffusion region.
2) Outer fringing capacitance.
3) Inner fringing capacitance (comes into picture only in absence of channel).

In simulation these capacitances and hence charge distribution are controlled by CKAPPA, CGS0, CGS1, CGD0, CGD1 and CGB0.

4.8 Implementation of Pulse Shaping Amplifier

Pulse Shaping Amplifier is also referred to as Shaper. In literature, large number of shaper has been discussed with different output shapes claiming low output noise performances. But all of them simply concentrated on reducing output noise, without mentioning how the shaper is going affect the actual incoming signal. It was evident that the sole goal was to improve the SNR, even if it meant loss of signal. For the current application, signal loss was not acceptable. Moreover all these sophisticated shapers use HPF as the first stage, followed by some number of LPFs. The incoming signal for the given application has its signal energy predominantly located at low frequencies, which makes the usage of HPF unsuitable for this application.

The final aim is to measure the DC value of the integrated current signal, so using HPF will defeat the very purpose and hence it has not been used. The aim of PSA is to provide gain to weak voltage output of CSP and provide higher attenuation to out of band noise signals. We are not providing gain in the shaper because of mainly two reasons:

1) We are imparting sufficient gain in LSA. and
2) We are using OTA (in unity feedback mode) instead of op-amp as the building block for the shaper.

Keeping all the above factors in mind, PSA has been implemented as a LPF of suitable order. In the proposed design OTA have been used instead of op-amp as basic building block, so output impedance is very high. Under such circumstances adding resistive

feedback network will not provide desired closed loop gain. So, unity gain has been chosen. The underlying OTA is folded cascode with following specification:

Parameter	Value
DC Open Loop Gain	48.5 dB
Band width	112 KHz
Unity Gain Frequency	30 MHz
Phase Margin	83.7 Degrees

Table 4.2: Parameters of Folded Cascode Amplifier

For the proper operation of a filter its underlying op-amp should have,

GBW or UGF = (cut-off frequency of filter) * (filter order)^2

= (200 KHz) * (16)

= 3.2 MHz

The overall filter architecture is shown in the following figure:

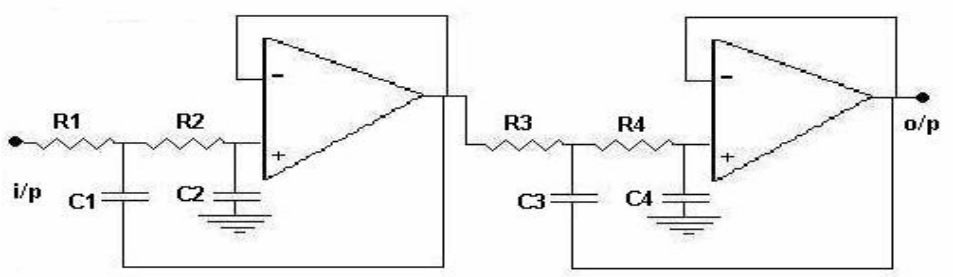

Fig 4.11: 4th order low pass filter architecture

Choice of cut-off frequency of LPF: Ideally one should use LPF with very low cut-off frequency, because output of CSP is expected to be DC like signal. But here LPF cut-off frequency has been chosen as 200 KHz. The reason for that is as follows:

It is known that, if a circuit has lesser BW, it will have higher rise time. For very small BW of shaper, the rise time is becoming very long and during that time output voltage of CSP is reducing significantly, due to discharge of integrating capacitor through the feedback element connected in parallel with it. This leads to significant loss of signal amplitude. As a result we are losing more due to signal loss compared to what we are gaining in terms of noise reduction. So, cut-off frequency of 200 KHz has been found to be best trade-off between avoiding signal loss and total output noise.

Different filter architecture has been studied for finding the most suitable architecture for the given problem. The desired features (in order of priority) for the required filter are:

i) Flat Pass band

ii) Constant Group Delay in the Pass band and

iii) High Roll-off Rate

The summary of the study of some well known filters is as follows:

Type of Filter	Pass band	Group Delay	Roll-off Rate
Butterworth	Maximally Flat (Best)	Constant (Better)	Medium
Bessel	Flat (Better)	Maximally Constant (Best)	Low
Chebyshev	Ripple in pass band (Bad)	Bad	High
Inverse Chebyshev	Pass band is neither flat nor rippled. Ripple in stop band	Worse	Higher
Elliptical	Ripple in pass band (Bad) and stop band	Worst	Highest

Table 4.3: Comparison of different filters

It is well known that Allpass filters (also known as delay equalizers) simply modifies the phase relationship between different frequency components of the input signal, so normally these filters are used in cascade with other filters to make the total group delay constant.

So, one of the proposal was to use Butterworth filter followed by Allpass filter. But the problem is that it will need a very high order Allpass filter to achieve overall constant group delay. So, this idea was dropped.

Some books had mentioned about a very interesting filter concept called "Transition Filters" [39, 40]. It is very well known that the type of response of any system is mainly decided by the locations of its poles and zeros. If some properties belonging to 2 different type of filters is required then intermediate poles and zeros of the 2 filters should be used, i.e. transition from one type of filter (D1) to another type of filter (D2).

$$P_{TR}(k) = P_{D1}^{m}(k) * P_{D2}^{1-m}(k)$$

Writing the above equation in polar form and separating magnitude and phase parts:

$$|P_{TR}(k)| = |P_{D1}(k)|^{m} * |P_{D2}(k)|^{1-m}$$

$$<P_{TR}(k) = <P_{D1}(k) - m\{<P_{D1}(k) - <P_{D2}(k)\}$$

Where k = 1, 2… N are the poles of the filters. "m" is the weighting factor & its value should be between 0 and 1.

If flat pass band and faster roll off is required simultaneously one can go for an intermediate filter having characteristics of both Butterworth and Chebyshev filter. Similarly, if flat pass band and constant group delay is a requirement then an intermediate filter having characteristics of both Butterworth and Bessel filter can be used. The transition filter of Bessel and Butterworth filter will be termed as Bessel-Butterworth filter henceforth. The Bessel-Butterworth filter will require comparatively higher order Bessel Filter. As a remedy, one can use Equiripple Delay filters [36]. Equiripple Delay filters gains advantage by distributing the permitted delay error uniformly over the pass band, rather than letting it increase monotonically towards the corner of the pass band (which is the case for Bessel filter) [36, 39, 46, 47].

Equiripple delay filters are good options as they are of lesser order and faster roll off rate compared to flat delay filters for the same cut-off frequency. But the "Q" associated with the poles is higher, which will cause peaking in time domain step response. So, finally Bessel-Butterworth filter was chosen. Number of values of weighting factor (m), were tried, before finalizing m = 0.5.

The pole locations & pole-Q, of 4th order Butterworth filter is as follows:

-0.3826834+j0.9238795, -0.3826834-j0.9238795, Q = 0.5412

-0.9238795+j0.3826834, -0.9238795-j0.3826834, Q = 1.307

The pole locations & pole-Q, of 4th order Bessel filter is as follows:

-2.8962106+j0.8672341, -2.8962106-j0.8672341, Q = 0.522

-2.1037894+j2.6574180, -2.1037894-j2.6574180, Q = 0.8055

The pole locations & pole-Q, of 4th order **Bessel-Butterworth filter**, for m=0.5, is as follows:

-1.6393+j0.5833, -1.6393-j0.5833, Q = 0.5307

-0.932645+j1.5875, -0.932645-j1.5875, Q = 0.9871

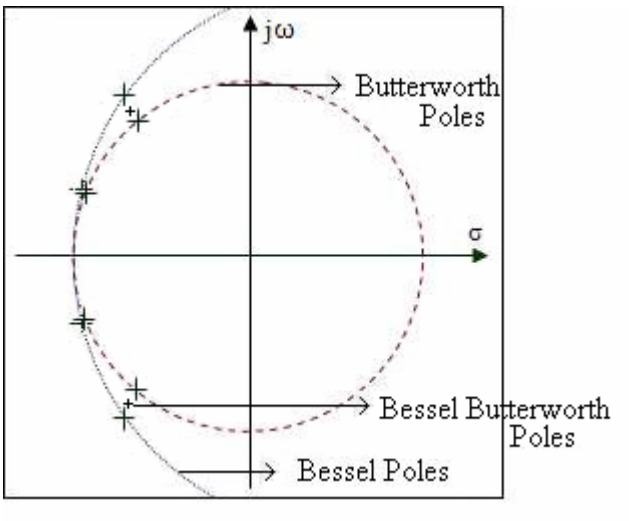

Fig 4.12: Location of Bessel-Butterworth poles w.r.t Bessel & Butterworth Poles

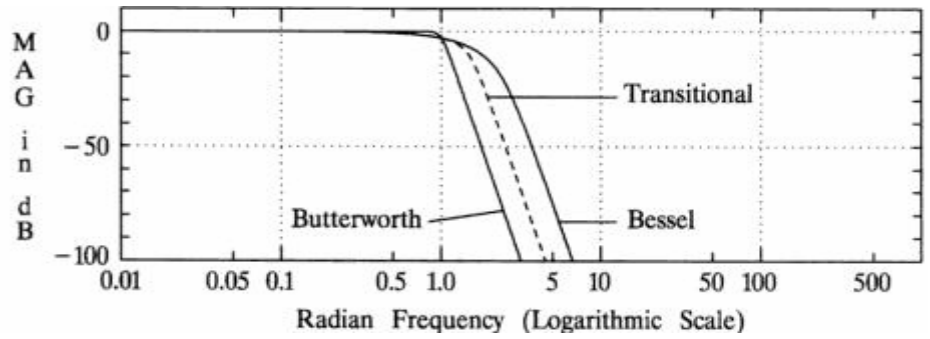

Fig 4.13: Magnitude response of Bessel-Butterworth filter wrt Bessel filter & Butterworth filter [39]

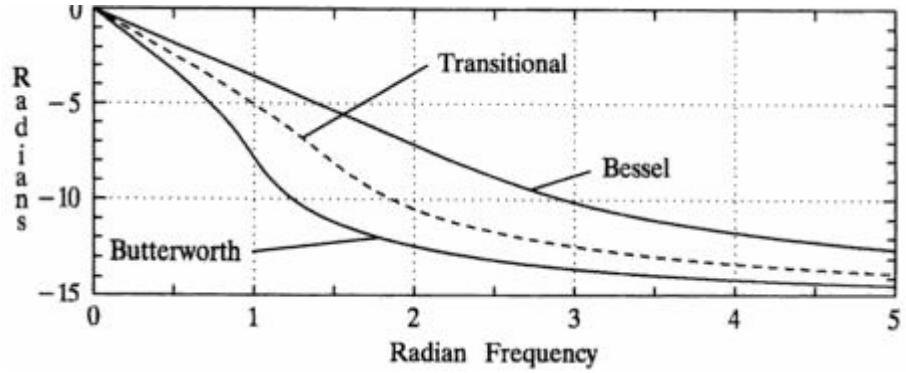

Fig 4.14: Phase response of Bessel-Butterworth filter wrt Bessel & Butterworth filter [39]

Finally, 2-staged, 4th order Bessel-Butterworth Filter was chosen, which as a whole gives a gain of 0.92

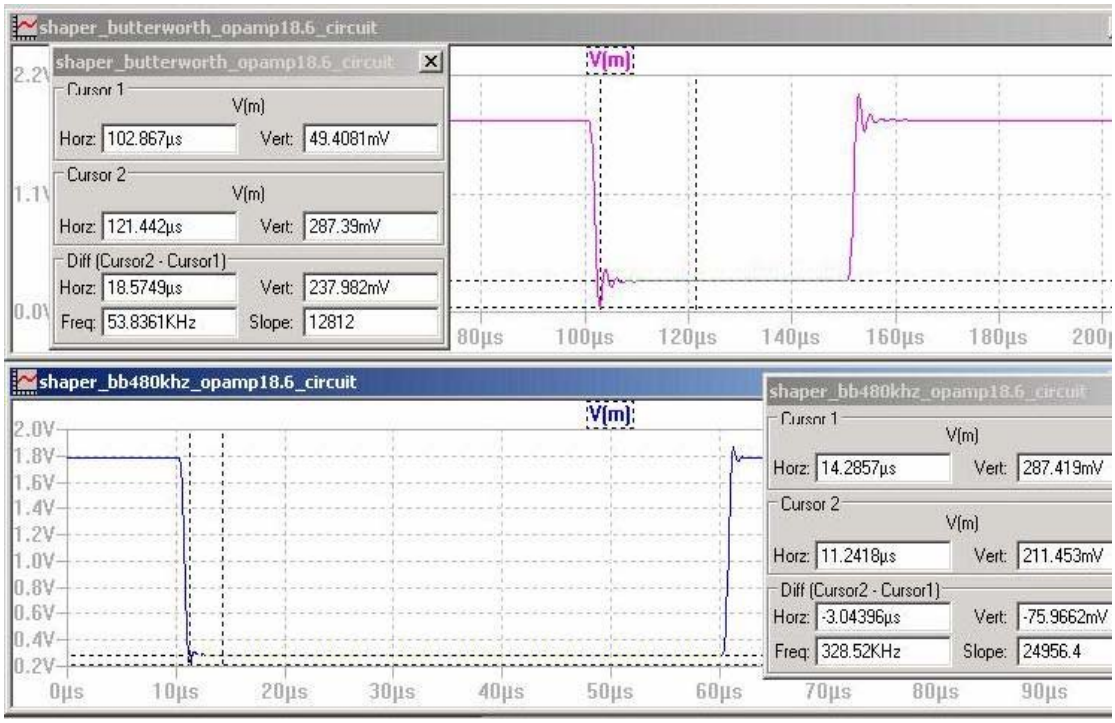

Fig 4.15: Outputs of Butterworth and Bessel-Butterworth filters

4.9 Why LPF in spite of having Peak Detector

It's a very obvious question that, "what is the need of having LPF when the output of amplifier (LSA), is anyway going to pass through the Peak Detector (which itself is an averaging device)?"

It is true that Peak Detector is an averaging device and hence it can suppress any random signal including noise. But an averaging device takes unacceptably long time to suppress the noise by desired degree, while a LPF of suitable order can do it in very less time. The reason for the same is as follows:

As per statistical property of random variables, if a measurement with standard deviation "s" is repeated "n" times then, the standard deviation in the mean value of measurement is "s / [square root (n)]". So, "n" measurements reduces effect of random variations (including noise), by a factor of square root of "n".

In continuous time domain interpretation of "n" is "n" time periods of the random signal.

If one wishes to suppress all noise signals beyond frequency (= f Hz), by at least 10 times (i.e. 20 dB), then total time required for that via averaging is 100/f, because the signal needs to be averaged over 100 cycles.

If the same is done via 1st order LPF, its cut-off frequency has to be f/10 Hz. So, the time constant for the LPF will be $10/2\pi f$. The output signal will almost reach its peak value in 10 time constants. Hence, total time required for LPF = $10*10/2\pi f = 100/2\pi f$.

If higher attenuation is required, in averaging technique time for averaging has to be increased, while in LPF, simply its order has to be increased.
Clearly LPF is **faster** than peak detector. Moreover, very high attenuation was required for out of band noise, so a LPF of 4th order (80dB/decade) has been used. If the same is done via averaging, total time required will be $10^8/f$, which is unacceptably very high.

4.10 Uniqueness in the work

1) The proposed approach is quite different from existing solutions (System level difference).
2) TG switch across C_{fb} has been used, with NMOS in sub-threshold.
3) Bessel-Butterworth filter is chosen as Low pass filter, with cutoff frequency, decided by essential band width of signal.
4) Subtractor at the output of peak detector has been proposed, which will remove DC offset, channel charge injected voltage and 1/f noise to great extent (Similar concept is used in CDS).
5) The intermediate amplifier stage is designed to serve dual purpose, of amplifying the weak voltage signal as well as providing level shifting to match output DC level of CSP with input DC level of shaper.

Chapter 5

Simulations

5.1 Procedure

For simulation purpose current pulses of amplitude 50nA were used. When current pulse was integrated across C_{fb} (= 50ff), it generated a voltage pulse of the amplitude 10.1mV which is then amplified by a factor of 15, by the amplifier. It also shifts the output DC level of CSP in order to match the required input DC level for the Shaper. Shaper is mainly 2 staged, 4th order Bessel-Butterworth Filter, which as a whole gives a gain of 0.9.

Overall transfer function of the system from input of CSP to output of Shaper is:

$T(s) = T_{CSP}(s) * T_{ampr}(s) * T_{filter}(s)$

$= R_{Mf}/(R_{Mf}C_{fb}s + 1) * A_{ampr}/(s + 2\pi*150*10^3) * A_{filter}/(s + 2\pi*150*10^3)$

The closed loop pole of CSP is near 1Hz. So, its transfer function can be approximated as:

$T_{CSP}(s) = 1/C_{fb}s$

$A_{ampr} = 15$; $A_{filter} = 0.9$

So, overall transfer gain at a frequency of 1 KHz ($s = 2\pi*10^3$) is:

$T(s = 2\pi*10^3) = 15 * 0.9 / (50 * 10^{-15} * 2\pi*10^3)$

$= 4.3 * 10^{10}$

Ratio of 1st harmonics (at 1 KHz) of filter output voltage (V(m)) & Detector Input current (I_{in}) = 207.28dB = $2.312 * 10^{10}$

Ratio remains almost same for higher harmonics also.

5.2 Actual Area Budget

Rough estimate of area consumed by different blocks is as follows:

CSP:	9265.4um^2
Transmission Gate Switch:	6.8um^2
Level Shifter cum Amplifier:	5.3um^2
Buffer:	108.9 um^2
2 Folded Cascode OTAs corresponding 4 filter stages:	217.8um^2
Total Area Excluding (Resistors and Capacitors):	9604.2um^2

The CSP is occupying a large fraction of area, as expected. Still, the total area is much less than what is available .i.e. 4,000,000um^2.

5.3 Resolution

Noise is always mentioned in terms of total input referred noise to make it independent of the gain of the following stages. Here the noise is been seen at the input of CSP which is current noise.

So, total input referred current noise is = 53.283 pA

This value is less than max noise current allowed (= 453 pA), which was derived from ENC specification earlier.

Min. signal current pulse amplitude (corresponding to X-Ray of energy 3 KeV) = 5nA

Worst case SNR = 5 nA / 53.283 pA = 93.84

A resolution of 3% was required, which translates into SNR = 100/3 = 33.4

So, required resolution is been achieved even in worst (smallest signal) case.

Making the noise calculations at output node, i.e. rechecking the resolution in terms of output referred noise, (area under v(onoise) curve):

Total Output Referred Noise = 2.64 mV

Minimum Signal Current expected = 5nA

Output Voltage corresponding to 5nA signal = 152.67 mV

So, for minimum signal resolution is = 2.64/152.67 * 100 = 1.73%

Simulated results for the overall circuit have been tabulated and compared with expected values in the following table:

Parameter	Expected Value	Simulated Value
Output of CSP (for Iin = 5nA)	10.1 mV	10 mV
Output of amplifier	176.75 mV	175.88 mV
Output of filter	154 mV	152.67 mV
I to V conversion ratio	$4.3 * 10^{10}$	$2.312 * 10^{10}$
Allowed Readout time	1 ms	0.012 ms
Resolution	3%	1.73%
Power Consumption	0.35 mW	0.2905 mW

Table 5.1: Comparison of expected and simulation results for overall system

5.4 Noise Statistics

It is a general practice to talk of noise as input referred noise to make it independent of the gain of the following stages. Also, input referred noise is a genuine parameter when we want to compare noise performance of different circuits or system i.e. it provides a fair basis for comparison.

In MOSFETs, normally the shot noise is negligible, so thermal noise and flicker noise are the main sources of noise. Out of these two, flicker noise is dominant at lower frequencies [34, 58]. The normal SPICE model for MOSFET doesn't take into account the flicker noise. To take its effect into .noise analysis, one needs to append the following parameters in the existing model [66, 68]:

Parameter	Meaning	Typical Value (NMOS/PMOS)
AF	Flicker Noise Exponent	1
KF	Flicker Noise Coefficient (The range for its reasonable values is 10^{-19} to 10^{-25})	$2.4 * 10^{-25}$ / $48 * 10^{-25}$ (Default value is 0).
NLEV	Noise equation selector	3
GDSNOI	Shot/Channel Noise Coefficient (Used with NLEV = 3)	2.5

Table 5.2: Flicker Noise Parameters

These parameters decide the flicker noise performance for any MOSFET. The values of these parameters are different for PMOS as well as NMOS. So, choosing proper values for them is crucial to get correct noise performance of any circuit.

The major contributor to output noise (as seen in simulation) were input PMOS transistor of CSP and NMOS reset transistor. The distribution of total output noise over the whole frequency band is as follows:

S. No.	Frequency Range	Output Referred Noise
1	1 Hz to 10 Hz	0.207031 mV
2	10 Hz to 100 Hz	0.211869 mV
3	100 Hz to 1 KHz	0.437464 mV
4	1 KHz to 10 KHz	1.155584 mV
5	10 KHz to 100 KHz	2.160746 mV
6	100 KHz to 1 MHz	0.811084 mV

7	1 MHz to 10 MHz	0.115625 mV
8	10 MHz to 100 MHz	0.099104 mV
9	100 MHz to 1 GHz	0.032950 mV

Table 5.3: Distribution of total noise over different frequency ranges

It is worth noting that, major noise contribution is from the frequency range 10 KHz to 100 KHz. The reason for this is small peaking in the noise plot in this frequency range, which can be seen in fig 5.7.

The methodology used for calculating the noise is as followed:

1) Noise analysis (.noise) is done in SPICE. Keep the frequency range for analysis equal to frequency of interest (Will be decided by cut-off frequency of filters used). For better results take more number of points between 2 decades (say, 100 points).
2) Noise values are exported to an excel sheet. The unit of noise values are $V/Hz^{1/2}$ (if voltage noise) and $A/Hz^{1/2}$ (if current noise).
3) The noise values obtained are squared. So, their units become V^2/Hz and A^2/Hz.
4) The next step is to integrate these values. There are different integration methods available like Trapezoidal method, Simpson's 1/3 Rule, Simpson's 3/8 Rule etc. Trapezoidal method has been used here for integration.
5) The integrated noise is having unit of V^2 and A^2. So, square root of the resulting integrated value is taken, which corresponds to desired voltage or current noise.
6) For getting input referred noise one can divide the output referred noise (or simply output noise) by the transfer gain of the preceding stages.

Input Referred noise with $R_{fb} = 2.42553 * 10^{-10}$ A.
Input Referred noise with NMOS in weak inversion and dummy NMOS switch on its both side, which are having (W/L) ratio half of the main NMOS = $9.2451 * 10^{-11}$ A.
Input Referred noise with NMOS in weak inversion, which is a part of TG switch = $3.7123 * 10^{-11}$ A.

5.5 Simulation Waveforms

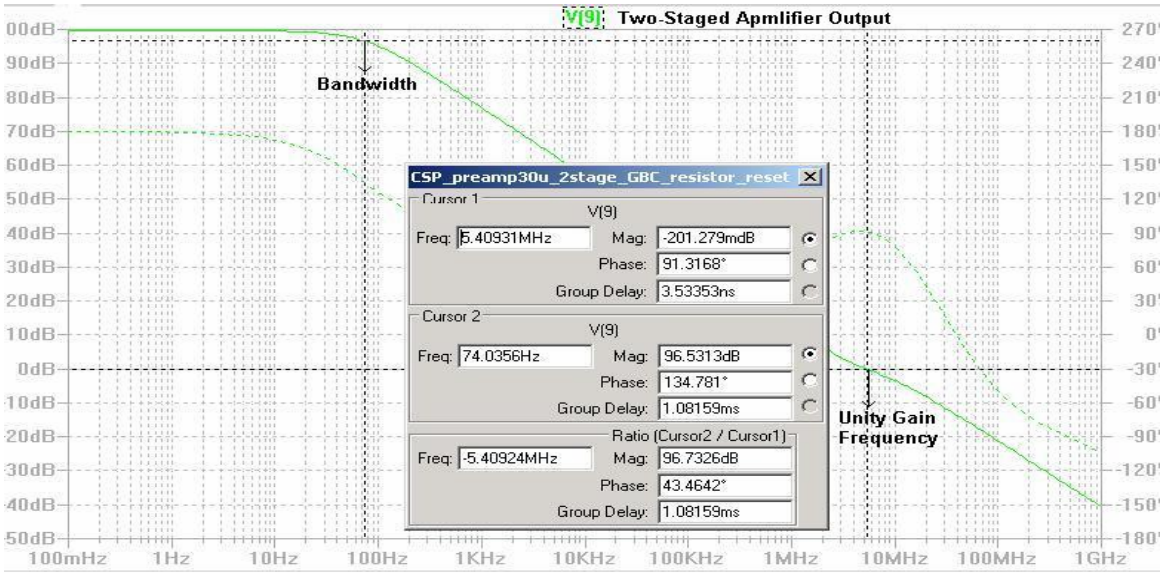

Fig 5.1: Frequency response of Two-stage amplifier used for CSP

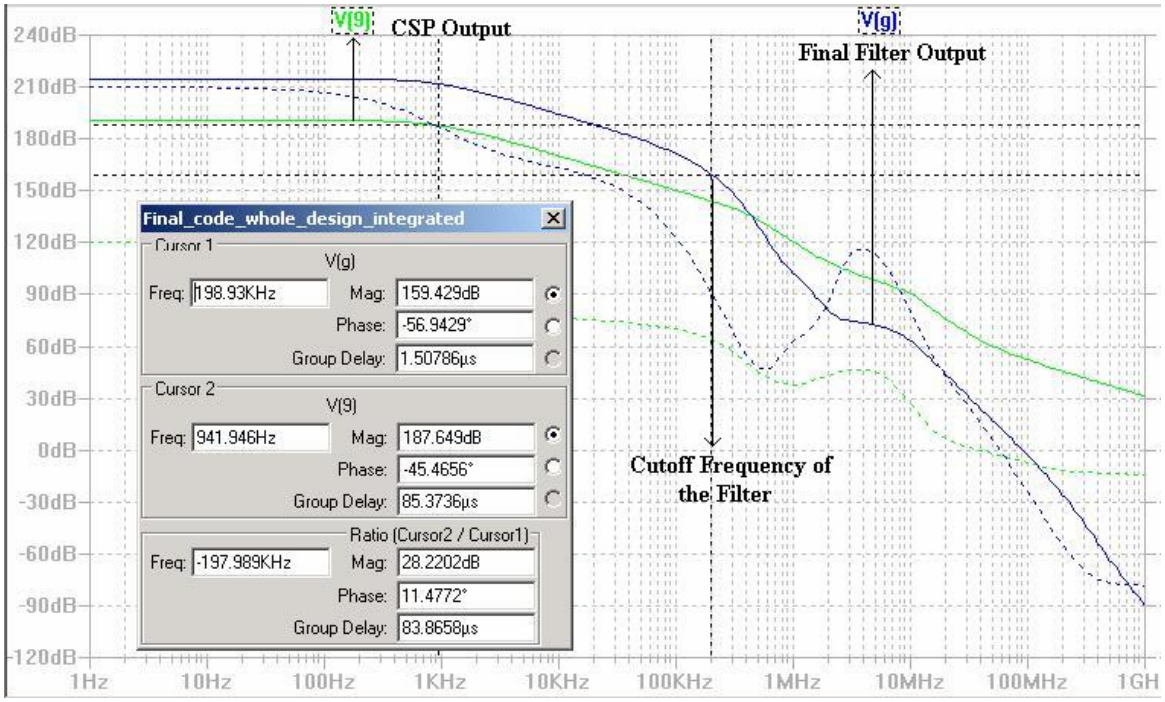

Fig 5.2: Frequency response of CSP, with NMOS in weak inversion (Integration starts from low frequencies). (Pole-Zero Doublet occurs at 4MHz & 1 MHz respectively).

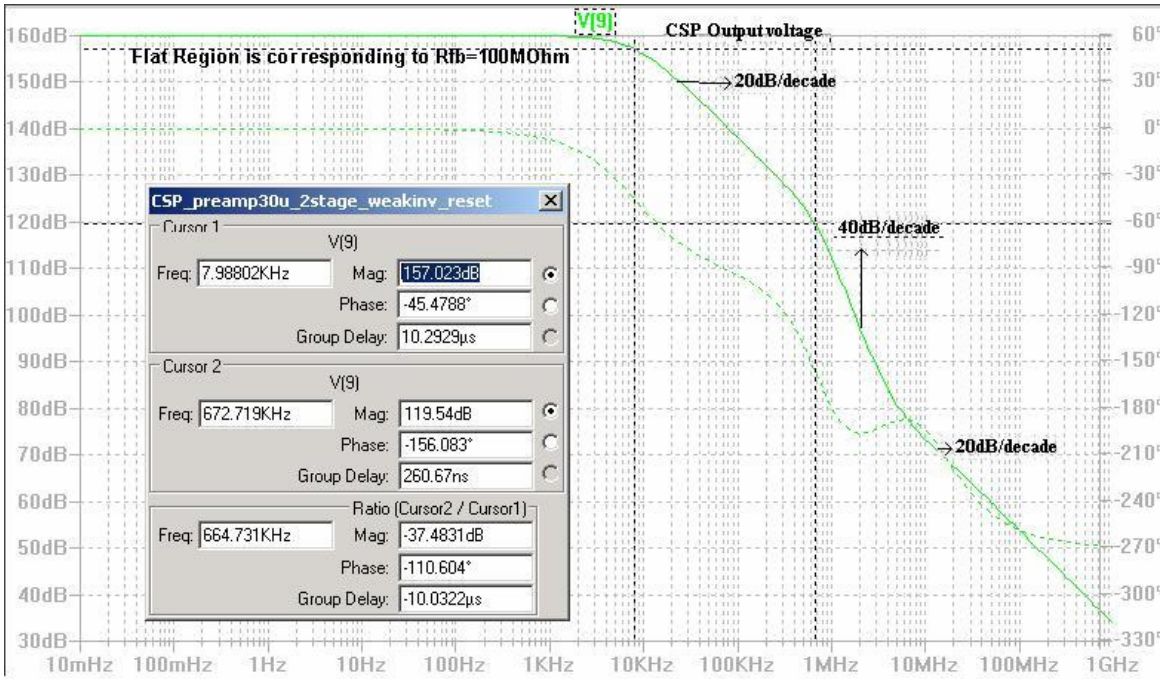

Fig 5.3: Frequency response of CSP with R_{fb} = 100 MΩ (Integration starts from comparatively high frequencies). (Pole-Zero Doublet occurs at 4MHz & 700 KHz respectively: Doublet moved towards lower frequency).

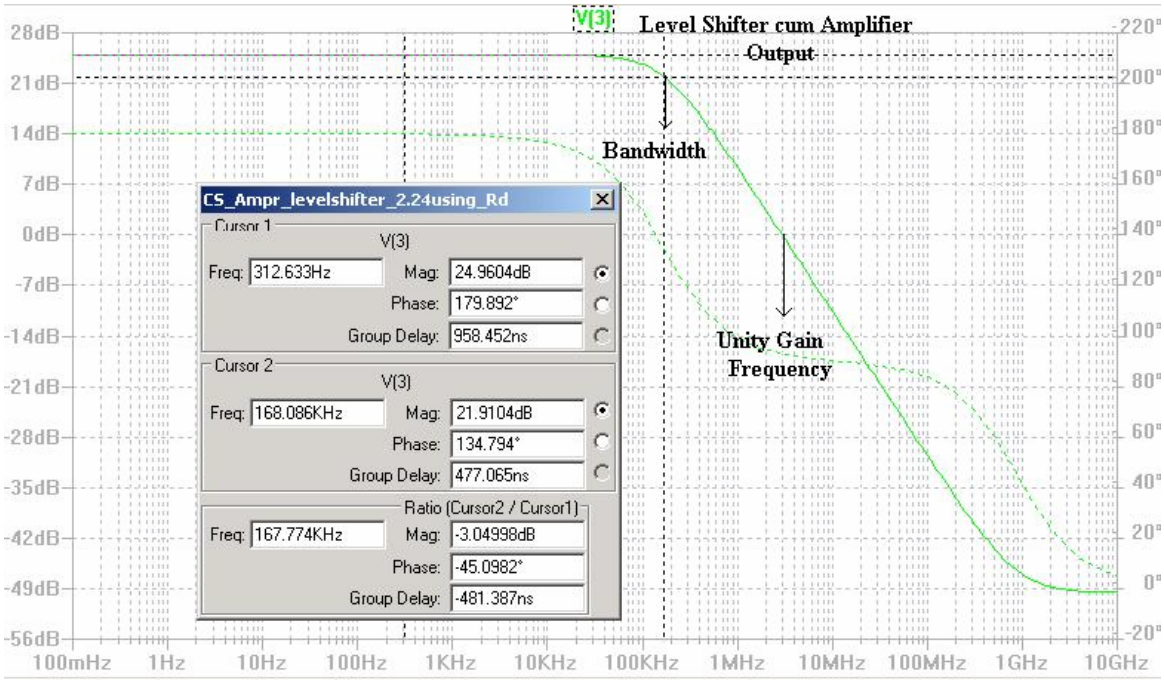

Fig 5.4: Frequency response of level shifter cum amplifier

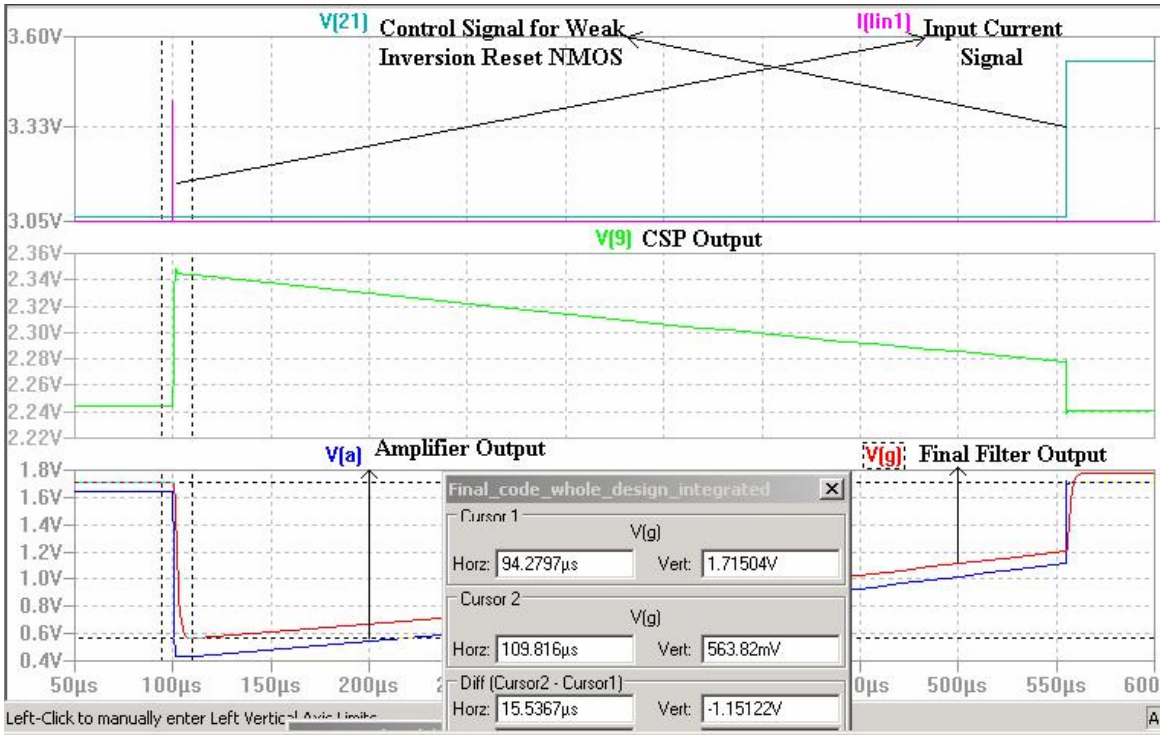

Fig 5.5: Output of Transient Analysis for overall circuit

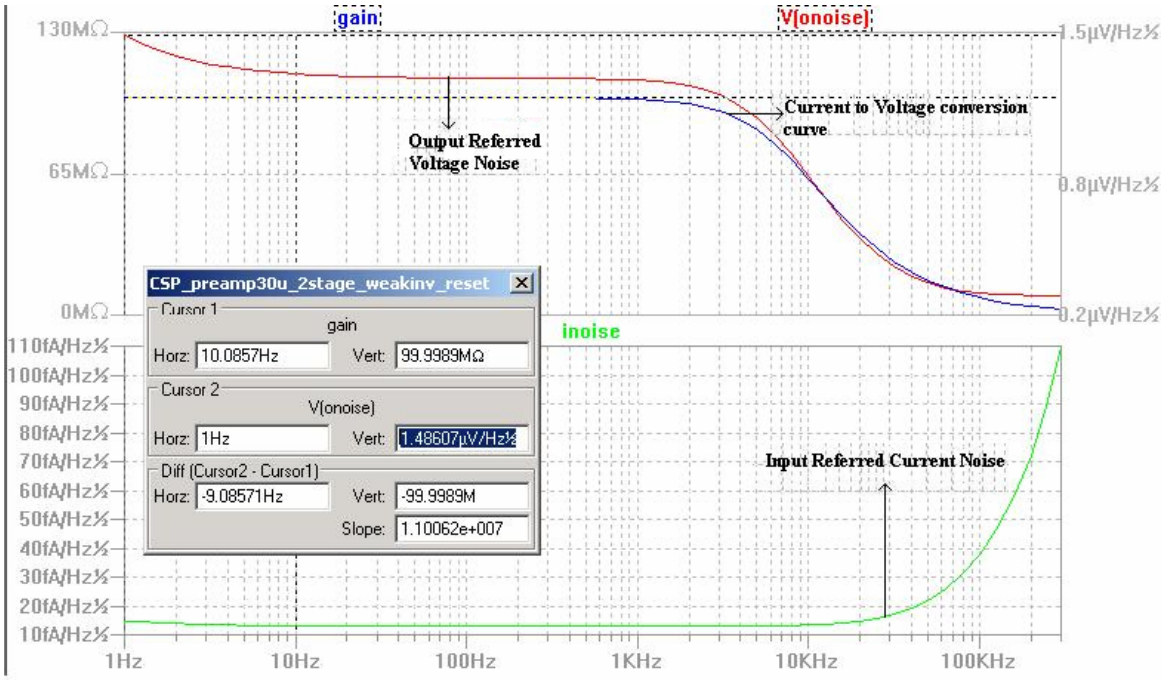

Fig 5.6: Output Noise Analysis of CSP with R_{fb} = 100 MΩ.

In R_{fb} thermal noise is the dominant source of noise, so V(onoise) curve is showing flat noise region after 10 Hz, which at higher frequencies is being limited by CSP Bandwidth.

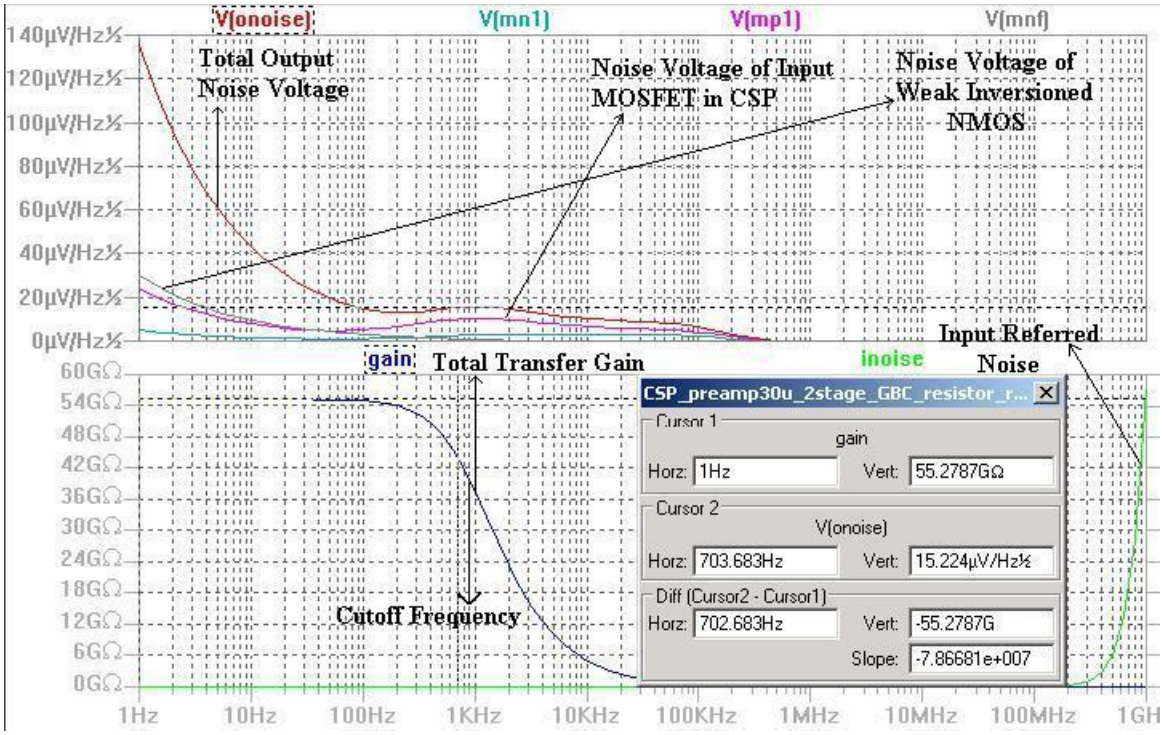

Fig 5.7: Output Noise Analysis of overall circuit

The noise curve is showing little peaking between 400 Hz to 200 KHz, due interaction between input capacitance of CSP and feedback resistor. Care should be taken in design of CSP to minimize this peaking and try to move this region towards the higher frequency end, which can be easily removed by LPFs.

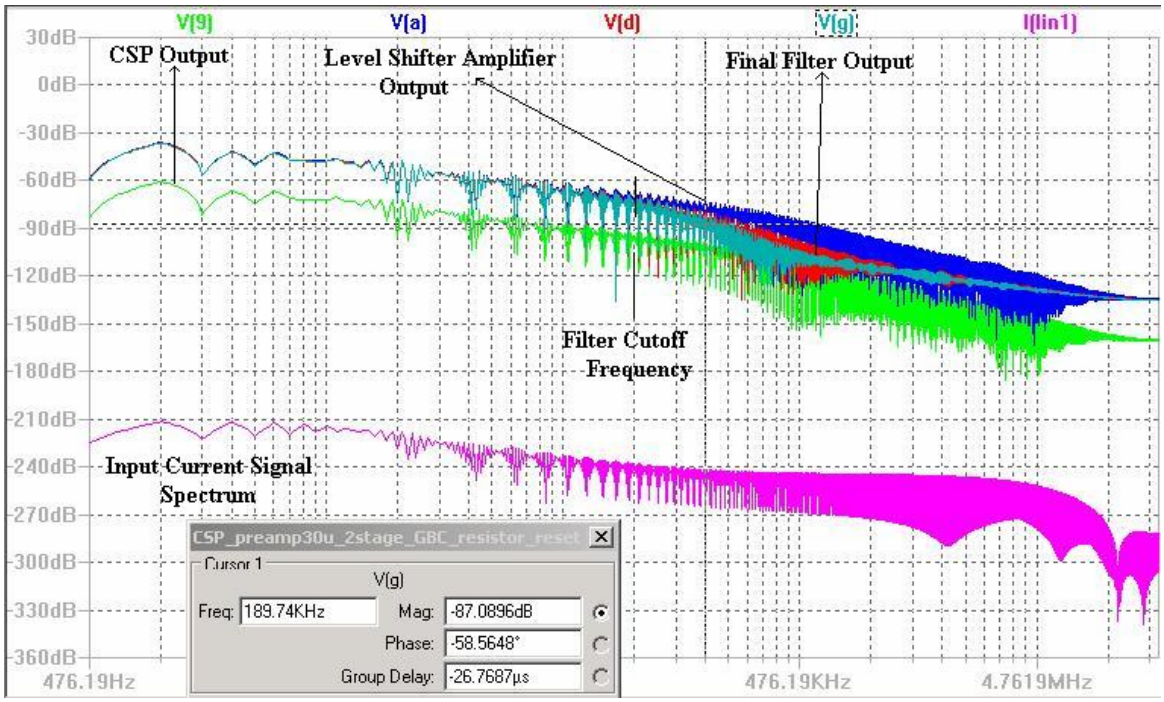

Fig 5.8: FFT of input, output and all other important intermediate signals

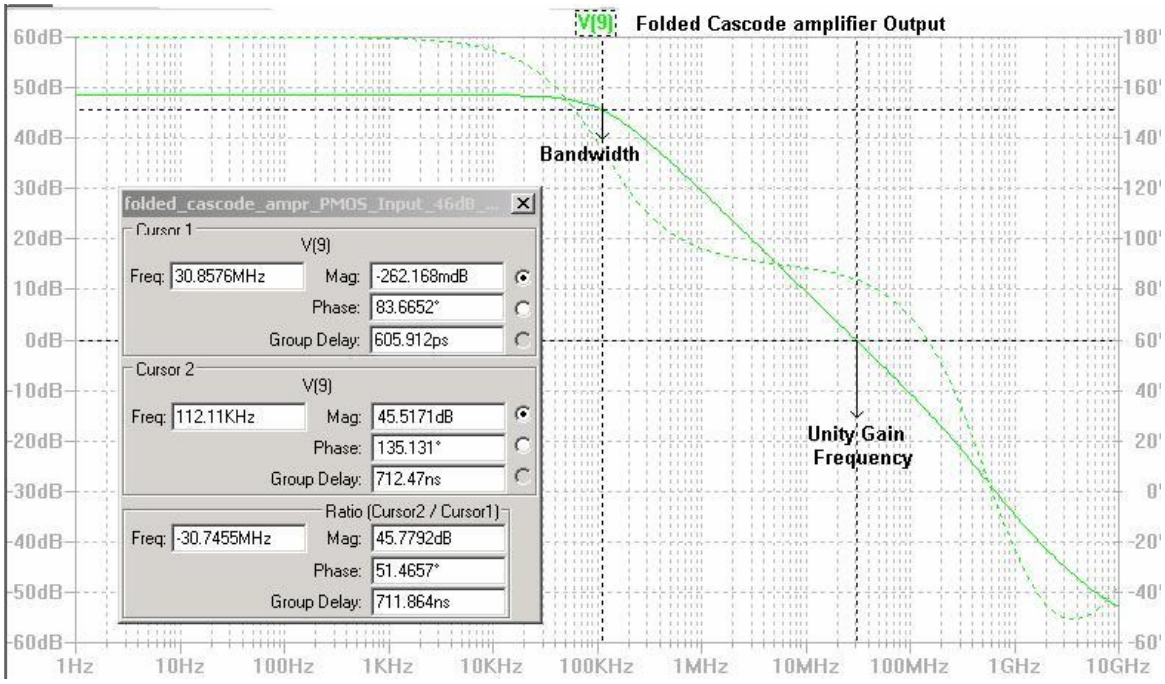

Fig 5.9: Frequency response of Folded Cascode Amplifier used for Shaper/Filter

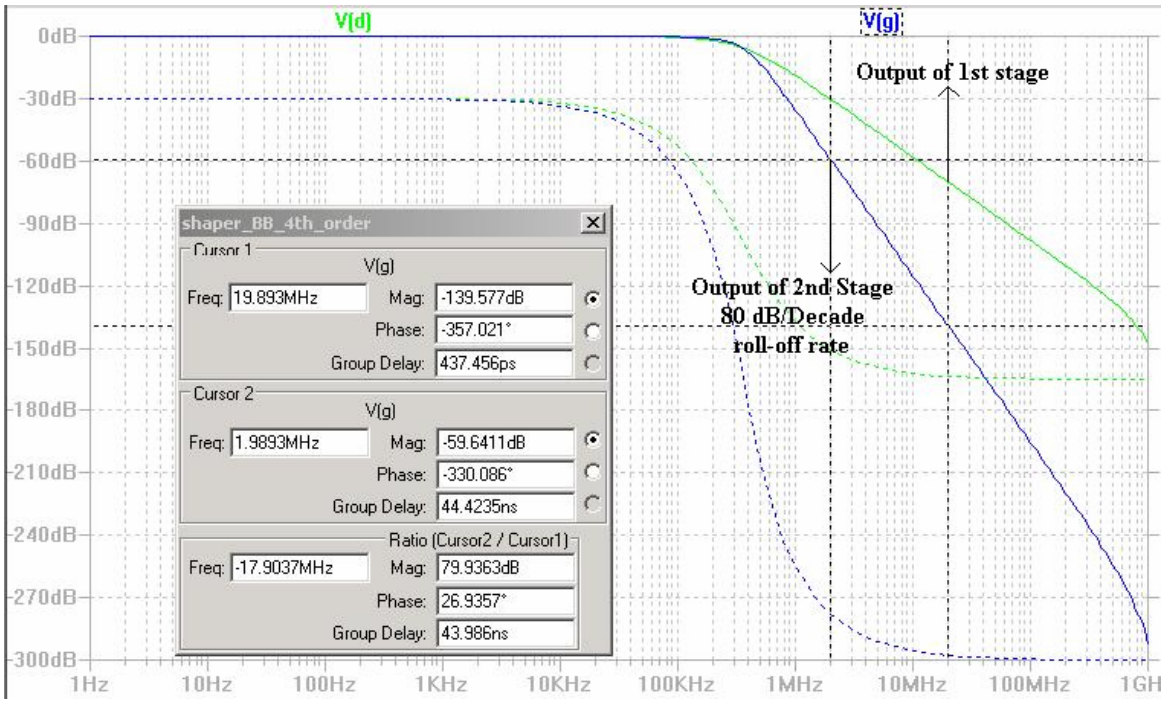

Fig 5.10: Frequency response of 2-staged, 4th order Bessel-Butterworth filter (Output of each stage is shown).

Chapter 6

Discussions and Conclusion

6.1 Discussion

6.1.1 Achievements

1) Noise contributed by transistor in weak inversion is far less than, even very high valued R_{fb}.
2) As per specs 3% resolution was required but the current design has been able to achieve much higher resolution (almost 1.7%).
3) 1,000 pulses/second/cm^2 is expected for the overall detector, but the design is currently supporting 83,000 pulses/second/channel (i.e. 20,75,000 pulses/second/cm^2, if X-Rays are uniformly distributed).
4) Bessel-Butterworth type filter is showing almost negligible overshoot in output.

6.1.2 Issues

1) The base amplifier for CSP should have good phase margin > 70 [25, 65].
2) Using R_{fb} is not suitable if the input signal spectrum is concentrated at low frequencies.
3) Value of C_{fb} plays a critical role in closed loop stability and dampness of the poles. Actually, value of C_{fb} is a tradeoff between output response, noise, stability, charge to voltage conversion ratio (sensitivity), effect of parasitic capacitors, coupling to next stage etc.
4) The real life amplifiers are OTAs and not Op-Amps, which causes lots of problems in designing circuits involving feedback. If characteristics close to an ideal Op-Amp is required, one must use number of other stages like level shifter, buffer etc followed by a high gain OTA.
5) Normally feedback network use to be resistive in nature. For the current design of CSP it is reactive. So, for deciding proper value of C_{fb} Root Locus should be used.
6) Channel Charge injection due to improper matching of PMOS & NMOS switches. Channel Charge Injection is 2nd order effect. Canceling this effect totally is a difficult task and normally requires a very complicated switching circuitry.
7) Tool (SPICE) related issue. Analysis was getting failed on many of the occasions, due to improper modeling of MOSFETs and/or due to Iteration limits reached.

SPICE uses linear equations only. To account for non-linear phenomena it uses to run the set of linear equations iteratively. If the calculation results don't converge within a fixed number of iterations, it shows an error message; "Analysis Failed: Iteration limits reached or Time step too small". Some of the proposed solutions available on internet suggest setting initial values for the variables using .NODESET command [112]. But in some of the cases even these solutions were not working.

8) There is a fundamental issue with modeling of charge in SPICE, due to which principle of "conservation of charge" fails in certain situations. Whenever this happens, voltage at some of the nodes keeps increasing linearly with time even in absence of any charge or current source. The reason for this effect is the assumption that capacitive elements in a MOSFET are reciprocal elements i.e. Cyz = Czy. But this assumption is wrong because in MOSFET charge at any one terminal, is a function of all the four terminal voltages i.e. voltages at drain, gate, source and bulk [54].

6.1.3 Points to Ponder

1) Design Strategy changes drastically with the application, which decides the corresponding design constraints. Low noise is normally desired for all the applications, but for the current design there were added constraints for area and power dissipation.
2) As the ASIC is meant for remote application it has to do all sort of pulse processing, on-chip itself, else it could have delegated some of its task to a more powerful computer.
3) Randomness of the input signal adds to further complications. If the shape of Input signal is known properly, its frequency spectrum will be known and hence one can choose better/tighter filter cutoff frequencies, which in turn will improve noise performance.
4) If time of incoming signal is known (like in medical applications) the control circuit for generating different control signals meant for different blocks, will be much accurate as well as simple. Also some modules can be put in sleep/standby mode when not used, which will save power.

6.1.4 Suggestions

1) Although keeping a high W & L for MOSFETs is desirable for reducing noise, especially for flicker noise. Keeping very high W & L can cause a noise peak at moderate frequencies, which contributes very high noise and hence degrades the noise performance.
2) Higher Roll-off (and hence higher order filter) is desirable to chop off the out of the band noise effectively. But care should be taken in choosing the number of stages, as too many stages can add more noise than what they remove.
3) CSP uses reactive feedback element, so use Root Locus for stability analysis and for choosing proper values of feedback elements.

6.1.5 Tradeoffs

1) Smaller size pixels have lesser noise, parasitic capacitance & charge collection time and hence higher resolution, but number of channels will increase and correspondingly total hardware will increase greatly.
2) Smaller C_{fb} provides higher sensitivity (current to voltage conversion ratio), but it increases kT/C noise and causes unstability.
3) Higher R_{fb} causes less low frequency signal loss and contributes lesser current noise, but it increases discharging time and hence lesser counting rate is possible.
4) Higher compensation capacitor (C_C) is required for better phase margin, but it decreases unity gain frequency greatly.
5) Settling time Vs Peak overshoot
6) Pass band Ripple Vs Roll-off rate for filters
7) Area Vs noise for CSP
8) High DC open loop gain (which implies small closed loop DC error) Vs Closed loop stability [52].

6.2 **Novelty**

1) The NMOS transistor of transmission gate is operated in weak inversion region during absence of the input current pulse. Due to weak inversion operation the NMOS shows a very high resistance (R_{ds}), so even the low frequency signal components flows through the integrating capacitor (C_{fb}). Apart from this, it is

also able to sink continuous DC leakage current up to 0.5 pA, which will otherwise saturate the C_{fb}.

2) The circuit is using Bessel-Butterworth low pass filter which can properly weight the requirements of almost zero (negligible) attenuation and constant group delay in the pass band. As a result better step response is obtained.
3) There is an innovation at system level. The overall architecture proposed is different from all other existing ASICs. Weak inversion NMOS transistor takes care of signal loss, Shaper (4^{th} order LPF) takes care of thermal noise and subtractor takes care of low frequency noise as well as charge injection. So, overall high resolution is achieved.

6.3 Future Work

1) The missing blocks mentioned in the proposed design can be undertaken.
2) Explore the charge injection pattern in Weak and Moderate Inversion.
3) Use advanced MOSFET model as well as some other powerful tool (like Cadence, Smash) to re-verify the results and optimize the design further.
4) Design some extra modules which will take care of abnormal situations, like increase in leakage current due to detector damage, protecting the circuit from high energy bursts etc.
5) Modify the existing design to achieve faster counting rates.
6) Layout of the whole design can be made which will estimate proper values of parasitic components and actual area consumed.

6.4 Conclusion

The design of an ASIC for detecting X-rays is presented. The proposed method has provided a novel architecture for radiation detector read out circuits to introduce low noise, while providing very high conversion ratio. The design is able to meet the crucial specifications of noise, power dissipation, area and count rate, which is validated by simulation results. It is anticipated that this design will be used for X-ray detection experiments in ISRO's second moon mission (Chandrayaan-II), once the remaining blocks are properly designed.

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Appendix-I

0.8um SPICE Model parameters [63]:

```
.MODEL CMOSN NMOS (                    LEVEL   = 49
+VERSION = 3.1          TNOM    = 27          TOX     = 1.55E-8
+XJ      = 2.5E-7       NCH     = 8E16        VTH0    = 0.641718
+K1      = 0.8346873    K2      = -0.042465   K3      = 12.7624417
+K3B     = -4.280204    W0      = 1.224565E-6 NLX     = 1E-8
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 2.3259952    DVT1    = 0.5694154   DVT2    = -0.1213192
+U0      = 518.874611   UA      = 4.751316E-10 UB     = 1.421977E-18
+UC      = 2.777785E-11 VSAT    = 1.089724E5  A0      = 0.7159742
+AGS     = 0.1226906    B0      = 1.260351E-6 B1      = 5E-6
+KETA    = -9.215897E-3 A1      = 0           A2      = 1
+RDSW    = 1.959338E3   PRWG    = -0.0156176  PRWB    = -3.095218E-7
+WR      = 1            WINT    = 1.794755E-7 LINT    = 1.270467E-7
+XL      = -2E-7        XW      = 0           DWG     = -2.481101E-8
+DWB     = 1.141719E-8  VOFF    = -0.0461706  NFACTOR = 1.2249987
+CIT     = 0            CDSC    = 8.997141E-5 CDSCD   = 0
+CDSCB   = 1.601628E-6  ETA0    = 7.778461E-3 ETAB    = -0.0159169
+DSUB    = 0.5668366    PCLM    = 0.6901938   PDIBLC1 = 0.0327512
+PDIBLC2 = 4.519874E-3  PDIBLCB = -6.055372E-5 DROUT  = 0.3916408
+PSCBE1  = 6.165635E9   PSCBE2  = 3.895022E-8 PVAG    = 8.271536E-3
+DELTA   = 0.01         MOBMOD  = 1           PRT     = 0
+UTE     = -1.5         KT1     = -0.11       KT1L    = 0
+KT2     = 0.022        UA1     = 4.31E-9     UB1     = -7.61E-18
+UC1     = -5.6E-11     AT      = 3.3E4       WL      = 0
+WLN     = 1            WW      = 0           WWN     = 1
+WWL     = 0            LL      = 0           LLN     = 1
+LW      = 0            LWN     = 1           LWL     = 0
+CAPMOD = 2             XPART   = 0.4         CGDO    = 1.82E-10
+CGSO    = 1.82E-10     CGBO    = 0           CJ      = 4.383428E-4
+PB      = 0.95242      MJ      = 0.440893    CJSW    = 3.672664E-10
+PBSW    = 0.1203645    MJSW    = 0.13661     PVTH0   = -0.0158267
+PRDSW   = -565.2171303 PK2     = -1.149287E-3 WKETA  = 1.719375E-4
```

```
+LKETA   = 2.545281E-4
* Noise parameters:
+ AF=1.0 KF=48E-25 NLEV=3.0 GDSNOI=2.5)

.MODEL CMOSP PMOS (                    LEVEL   = 49
+VERSION = 3.1          TNOM    = 27          TOX     = 1.55E-8
+XJ      = 2.5E-7       NCH     = 5E16        VTH0    = -0.8875042
+K1      = 0.3369914    K2      = 0.0371665   K3      = 19.1068598
+K3B     = -4.9002263   W0      = 2.995004E-6 NLX     = 2.015444E-7
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 2.7785049    DVT1    = 0.5598794   DVT2    = -0.0832108
+U0      = 206.4070087  UA      = 2.442882E-9 UB      = 5.717441E-20
+UC      = -5.59977E-11 VSAT    = 1.942916E5  A0      = 0.6065878
+AGS     = 0.0158204    B0      = 3.358896E-6 B1      = 5E-6
+KETA    = 2.311465E-3  A1      = 0           A2      = 1
+RDSW    = 2.129402E3   PRWG    = 1.262219E-3 PRWB    = -0.0228669
+WR      = 1            WINT    = 1.793093E-7 LINT    = 6.008561E-8
+XL      = -2E-7        XW      = 0           DWG     = -1.882411E-8
+DWB     = 2.402293E-8  VOFF    = -0.047527   NFACTOR = 1.1406197
+CIT     = 0            CDSC    = 2.771735E-6 CDSCD   = 1.041857E-5
+CDSCB   = 3.087982E-4  ETA0    = 0.0703497   ETAB    = -6.11347E-4
+DSUB    = 0.3547864    PCLM    = 5.063164    PDIBLC1 = 1.071833E-4
+PDIBLC2 = 0.0215228    PDIBLCB = 0.1         DROUT   = 0.0525797
+PSCBE1 = 1.944839E9    PSCBE2 = 2.320666E-9  PVAG    = 0.0925467
+DELTA   = 0.01         MOBMOD = 1            PRT     = 0
+UTE     = -1.5         KT1     = -0.11       KT1L    = 0
+KT2     = 0.022        UA1     = 4.31E-9     UB1     = -7.61E-18
+UC1     = -5.6E-11     AT      = 3.3E4       WL      = 0
+WLN     = 1            WW      = 0           WWN     = 1
+WWL     = 0            LL      = 0           LLN     = 1
+LW      = 0            LWN     = 1           LWL     = 0
+CAPMOD = 2             XPART   = 0.4         CGDO    = 2.91E-10
+CGSO    = 2.91E-10     CGBO    = 0           CJ      = 6.184038E-4
```

+PB = 0.8945284 MJ = 0.479411 CJSW = 4.379993E-10

+PBSW = 0.99 MJSW = 0.4208291 PVTH0 = 0.0492405

+PRDSW = -1.3E3 PK2 = 1.348997E-3 WKETA = -7.720116E-3

+LKETA = -8.9419E-3

* Noise parameters:

+ AF=1.0 KF=2.4E-25 NLEV=3.0 GDSNOI=2.5)

Appendix-II

Dedicated to Charge Cancellation

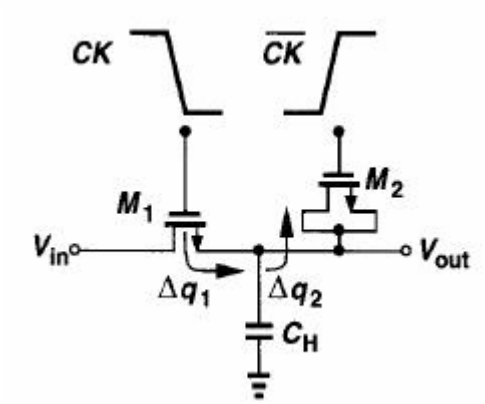

Fig A2.1: Charge cancellation using dummy switch [19]

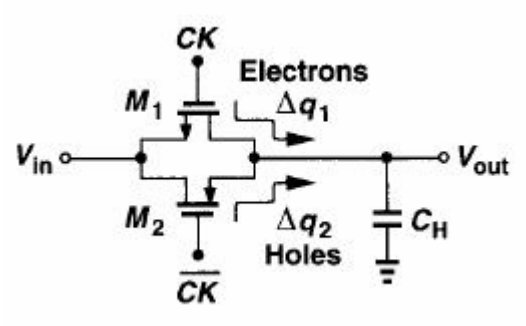

Fig A2.2: Charge cancellation using transmission gate [19]

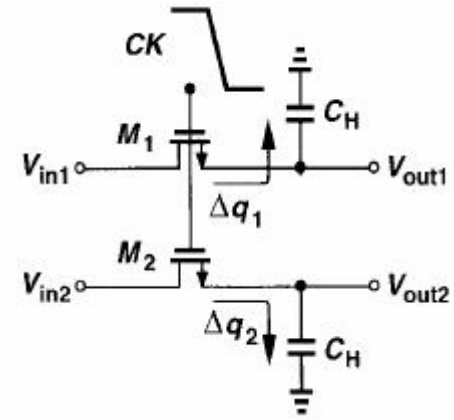

Fig A2.3: Charge cancellation using differential sampling [19]

Appendix-III

Dedicated to Transition Filters [39, 40]

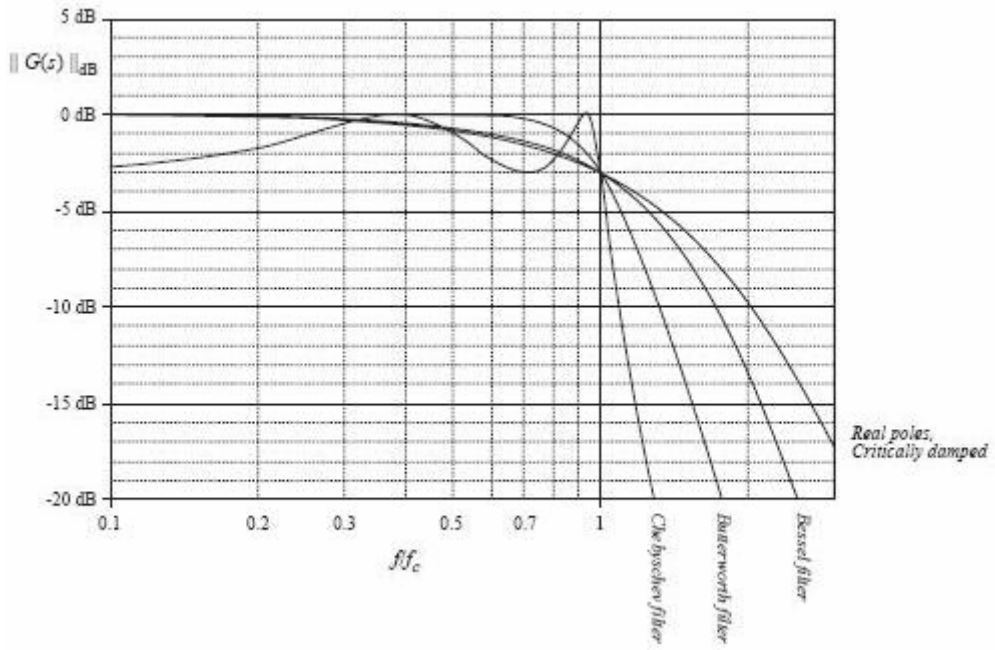

Fig A3.1: Frequency Response of Bessel, Butterworth and Chebyshev filters [39, 40].

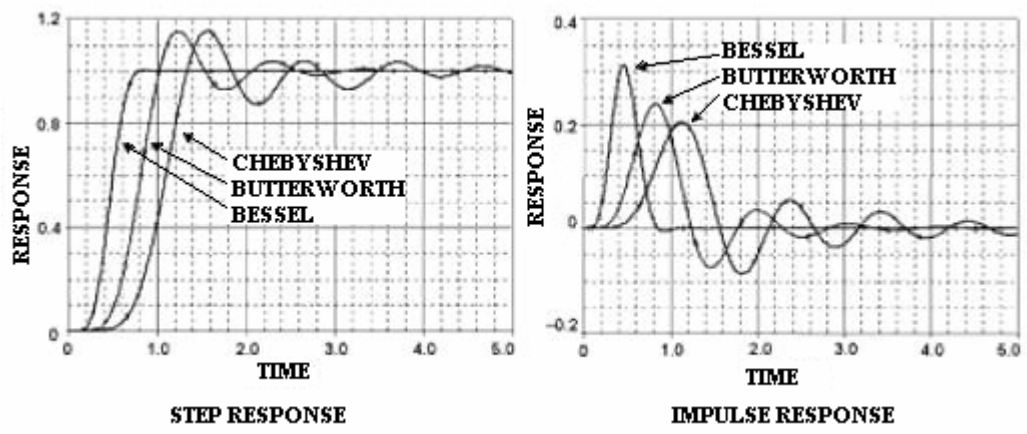

Fig A3.2: Step and Impulse Response of Bessel, Butterworth and Chebyshev filters [39]

Calculations are shown for Bessel-Butterworth and Equiripple Delay-Butterworth filters with m = 0.8 (lesser weight to Butterworth response).

The pole locations & pole-Q, of 8th order Butterworth filter is as follows:

-0.195+j0.981, -0.195-j0.981, Q = 2.56

-0.556+j0.831, -0.556-j0.831, Q = 0.9

-0.831+j0.556, -0.831-j0.556, Q = 0.6

-0.981+j0.195, -0.981-j0.195 Q = 0.51

The pole locations & pole-Q, of 8th order Bessel filter is as follows:

-2.839+j6.354, -2.839-j6.354, Q = 1.225

-4.368+j4.414, -4.368-j4.414, Q = 0.711

-5.205+j2.616, -5.205-j2.616, Q = 0.56

-5.588+j0.868, -5.588-j0.868 Q = 0.506

So, resultant pole locations & pole-Q, of 8th order **Bessel-Butterworth filter**, for m=0.8, is as follows:

-1.7311+j4.3924, -1.7311-j4.3924, Q = 1.364

-2.9124+j3.1774, -2.9124-j3.1774, Q = 0.74

-3.6123+j1.9288, -3.6123-j1.9288, Q = 0.567

-3.9473+j0.6472, -3.9473-j0.6472 Q = 0.5067

The pole locations & pole-Q, of 8th order Equiripple Delay filter is as follows:

-0.534+j2.476, -0.534+j2.476, Q = 2.37

-0.722+j1.814, -0.722+j1.814, Q = 1.352

-0.792+j1.106, -0.792+j1.106, Q = 0.8588

-0.819+j0.371, -0.819+j0.371, Q = 0.549

So, resultant pole locations & pole-Q, of 8th order **Equiripple Delay -Butterworth filter**, for m=0.8, is as follows:

-0.4369+j2.0575, -0.4369-j2.0575, Q = 2.41

-0.6979+j1.559, -0.6979-j1.559, Q = 1.224

-0.8178+j0.9838, -0.8178-j0.9838, Q = 0.7822

-0.853+j0.3405, -0.853-j0.3405 Q = 0.5384

It can be observed very easily that, due to rippled delay in pass band of Equiripple Delay Filter, it is having higher Q values associated with each pole. So, Equiripple Delay Filters has higher roll-off rate compared to Bessel Filters.

Appendix-IV

Dedicated to weak inversion operation [22, 64, 73]:

Operation is said to be in weak inversion region if, the surface potential is greater than Fermi potential, but its value is less than twice the Fermi potential.

$$\phi_F < \phi_S < 2\phi_F$$

For Weak Inversion, the charge in the channel is much lower and drift-current decreases (the channel resistance is high). However there is a concentration gradient in the channel that causes diffusion current, like a BJT [22, 73].

Large Signal Model for Weak Inversion:

The electrons in the substrate at the source side can be expressed as:

$$n_p(0) = n_{po}\exp\left(\frac{\phi_S}{V_t}\right)$$

The electrons in the substrate at the drain side can be expressed as:

$$n_p(L) = n_{po}\exp\left(\frac{\phi_S - vDS}{V_t}\right)$$

So, the drain current due to diffusion is:

$$i_D = qADn\left(\frac{n_p(L) - n_p(0)}{L}\right) = \frac{W}{L}qXD_n n_{po}\exp\left(\frac{\phi_S}{V_t}\right)\left[1 - \exp\left(-\frac{vDS}{V_t}\right)\right]$$

Where, X is the thickness of the region where i_D flows.

Writing the same equation in terms of Gate-Source & Drain-Source voltages

$$i_D = \frac{W}{L}I_t\exp\left(\frac{vGS - VT}{nV_t}\right)\left[1 - \exp\left(-\frac{vDS}{V_t}\right)\right]$$

Where, n =1.5 to 3 (depends on type of junction); V_t is thermal voltage; and

$$I_t = qXD_n n_{po}\exp\left(\frac{k2}{V_t}\right)$$

Small Signal Model for Weak Inversion:

$$gm = \frac{diD}{dvGS}\Big|_Q = I_t\frac{W}{L}\frac{1}{nV_t}\exp\left(\frac{vGS - VT}{nV_t}\right)\left(1 + \frac{vDS}{V_A}\right) = \frac{ID}{nV_t} = \frac{qID}{nkT} = \frac{ID}{Vt}\frac{Cox}{Cox + Cjs}$$

$$gds = \frac{diD}{dvDS}\Big|_Q \approx \frac{ID}{V_A}$$

The boundary between weak and strong inversion found via the g_m/I_D comparison:

$$g_m/I_D = \frac{\sqrt{2\beta I}}{I} = \frac{2}{[V_{GS} - V_T]}$$

Transition occurs when g_m/I_D is equal for both strong and weak inversion regions:

$$\frac{2}{[V_{GS} - V_T]} = \frac{1}{nV_t} \quad ==> \quad V_{GS} - V_T = 2nV_t \equiv V_{Overdrive}$$

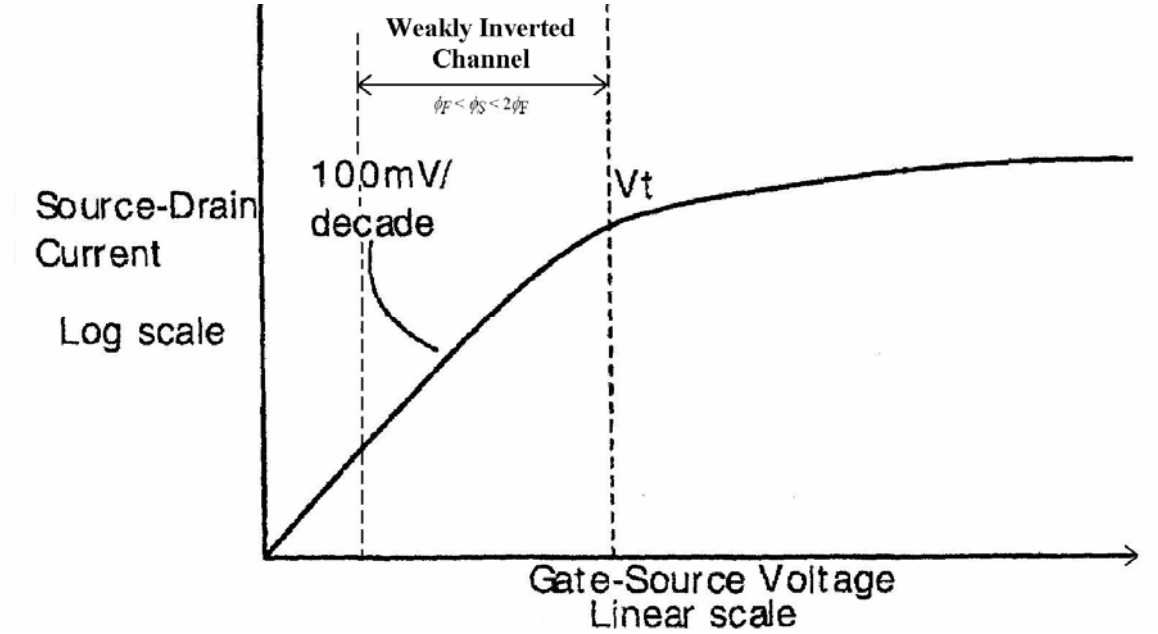

Fig A4.1: Variation of operating region as a function of Gate-Source Voltage (Slant region between 2 dotted lines is showing the weak inversion region) [73]

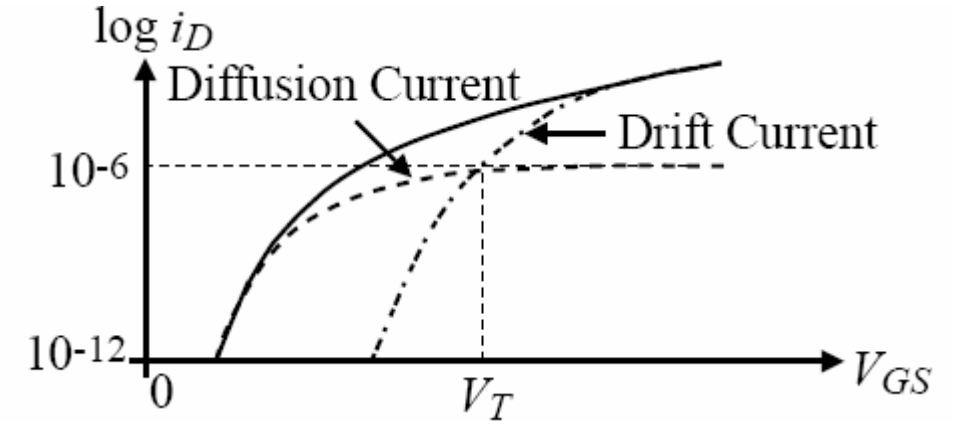

Fig A4.2: Distribution of currents in weak inversion region [73]

Appendix-V

Dedicated to overall ROIC [6, 25, 65]:

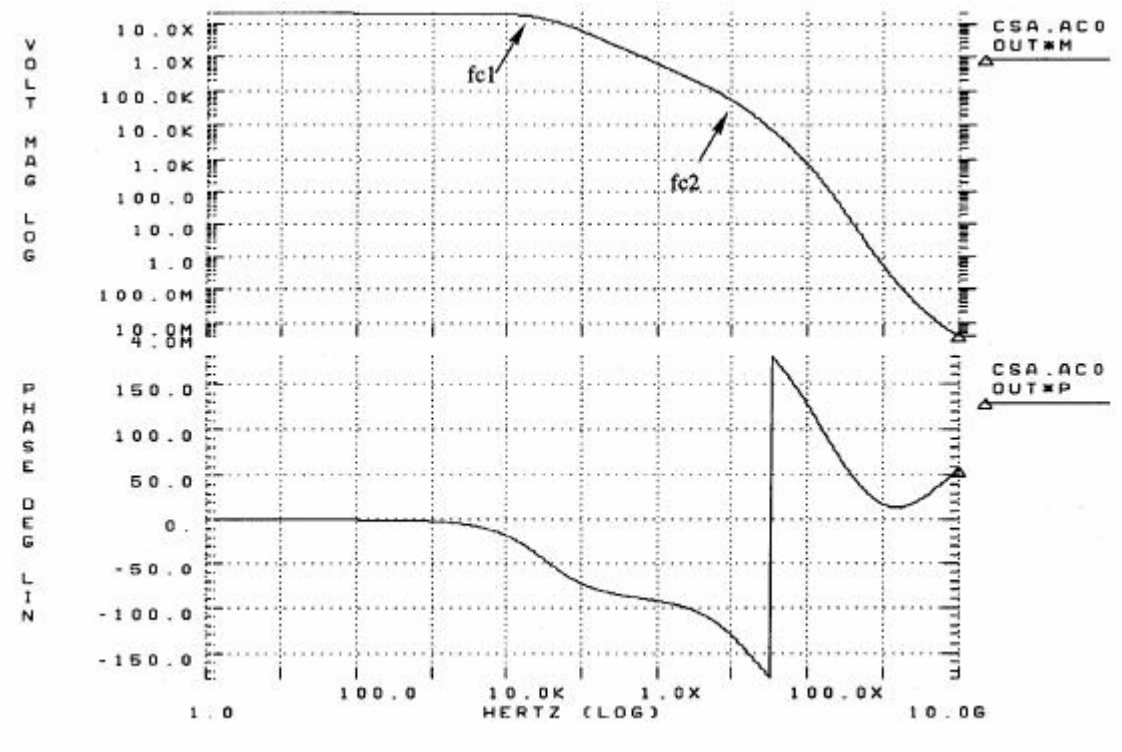

Fig A5.1: Closed Loop Magnitude and Phase response of CSP of one of the manufactured chip [65].

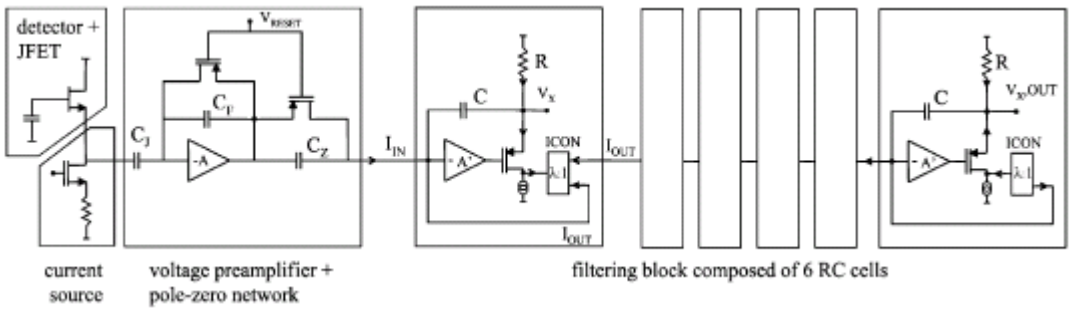

Fig A5.2: Single analog channel for the readout chip [6]

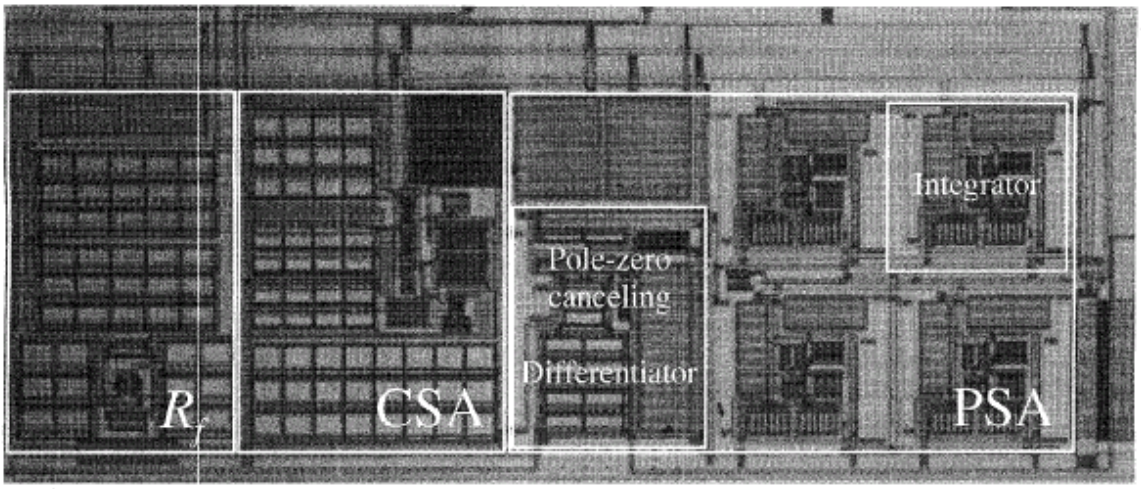

Fig A5.3: Microphotograph of layout of manufactured CSP-PSA [65].

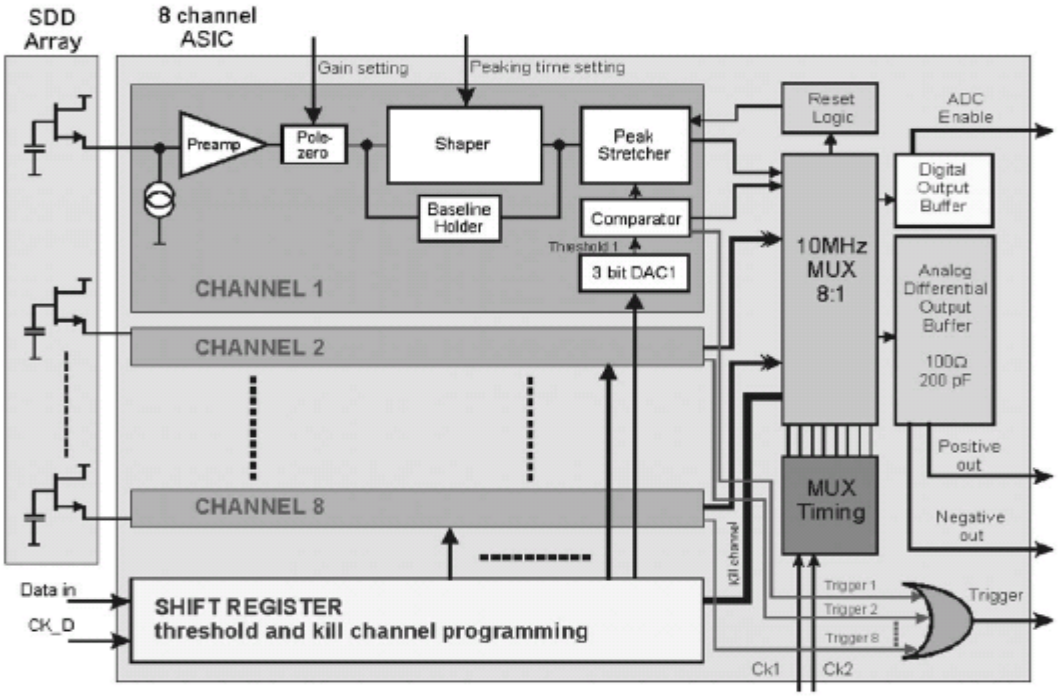

Fig A5.4: Layout of overall 8-channel Readout chip [6]

Appendix-VI

Dedicated to low noise approaches:

Some of the thumb rules to reduce noise are as follows:

1) Use BJTs over MOSFETs to reduce 1/f noise [4, 5, 22, 34, 58].
2) Use PMOS over NMOS to reduce 1/f noise [4, 5].
3) Use Chopper Stabilization Concept [22, 111] or CDS Technique to cancel 1/f noise [61, 62, 108-111].
4) Keep the gain of the first stage as high as possible and noise as low as possible. The noise from the subsequent stage will be divided by the gain of the previous stages, when referred at the input [1].
5) Keep gm high for the input transistors and low for load transistors. This will reduce total thermal noise and 1/f noise [1, 4].
6) Choose the input differential amplifier topology such that it has minimum number of terminal transistors, as they contribute maximum amount of noise [19].
7) Increase the capacitance to smoothen out noise. So, keep W and L high for both input and load transistors [4].
8) Designing for high output voltage swing provides better performance in terms of SNR, Speed and power dissipation [107].
9) Keep the interconnect length between different modules; especially from detector sensor to first stage of readout circuit should be as small as possible. This reduces stray capacitance as well as noise.
10) Match X-Ray detector sensor capacitance with input capacitance of first stage of readout circuit. Higher the mismatch, higher the noise [74, 75].
11) Keep the power consumption of the system low. Also dissipate the generated power efficiently, to maintain low operating temperature, which will ensure lesser thermal noise. Use cooling, if possible.

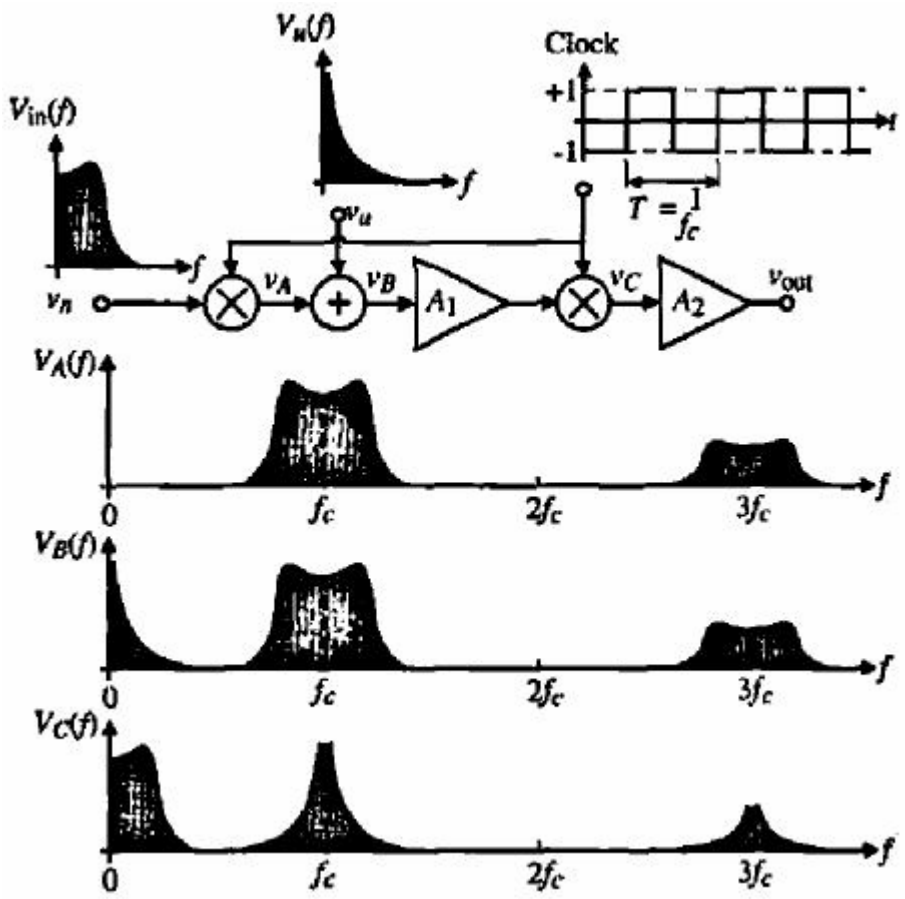

Fig A6.1: Chopper Stabilization concept to remove undesired signal V_u, from desired signal V_{in} [22].

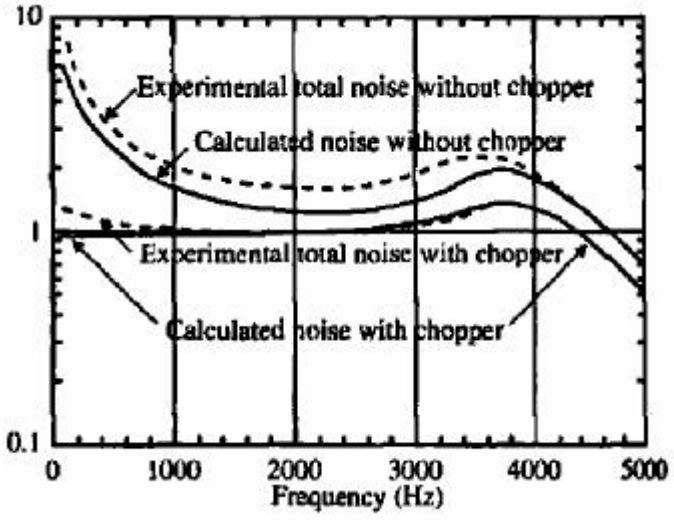

Fig A6.2: Noise Performance with and without chopper [22].