A Novel Architecture

For a CMOS Low Noise Amplifier at 2.4 GHz

by

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Declaration

This is to certify that

(i) the thesis comprises my original work towards the degree of Master of Technology in Information and Communication Technology at DA-IICT and has not been submitted elsewhere for a degree,

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This is to certify that the thesis work entitled " Design of a CMOS LNA at 2.4 GHz " has been carried out by Anuradha Ray (200311018) for the degree of Master of Technology in Information and Communication Technology at this Institute under my/our supervision.

Thesis Supervisor(s)

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I dedicate this work to my grandfather, Late Shri Shambhunath Ray, who always encouraged me to excel in professional life and be a good human being.

Contents

Abstract

Radio frequency design has been one of the major research areas in the recent past. Emergence of several Wireless Communication standards has demanded availability of different analog blocks for use in transceivers with different constraints, imposed by the nature of application. Particularly, lot of research has been carried out in CMOS technology, due to its low cost nature.

LNA is one of the most important building blocks in the front end of the wireless communication systems. It determines the noise performance of the overall system, as it is the first block after the antenna. With technology scaling, the transistor's cut off frequency continues to increase, which is desirable for improving the noise performance of CMOS circuit. Some other advantages like low cost, high level of integration motivates research of RF modules using CMOS technology. In recent years valuable research is done on CMOS LNA design in submicron technologies: from topology investigation to various new ideas on improvement of low power consumption, low noise figure, high gain, smaller space and low supply voltage.

In this thesis, a new LNA architecture is reported, that consumes less power compared to other existing architectures, while providing the same gain, noise figure, CP_{-1dB} and IIP3 figures. The new architecture achieves this better performance by combining the beneficial properties of two existing architectures – Lee's inductive input stage, and the current-reuse (or the CMOS inverter amplifier) architecture. Detailed design procedures, and Spice simulation results are presented in the thesis, along with a brief survey of noise sources in MOSFETs, and a literature survey of existing LNA architectures.

List of Principal Symbols and Acronyms

q	Electronic charge(1.6×10^{-19}C)
ω_T	Cut off frequency of MOSFET
L	Inductance
C	Capacitance
G	Conductance
B	Admittance
E	Electric field
I	Current
k	Boltzmann's constant
Y	Admittance
Z	Impedance

Other minor symbols are defined at first occurrence; where necessary some symbols are redefined in the text.

DC	Direct Current
RMS	Root mean square
MOSFET	Metal oxide semiconductor field effect transistor
CMOS	Complementary MOS
NF	Noise figure
RF	Radio frequency
IC	Integrated Circuit

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Chapter 1

Introduction

1.1 General

With the development of the personal communication market, the design of the low power RF integrated circuit becomes more and more important. Previously all RF circuits were implemented using gallium arsenide (GaAs) or bipolar junction transistor (BJT) technologies. But with CMOS process development it is becoming a better option for low power design. As the cutoff frequency of CMOS device has increased above a few tens of GHz, CMOS circuits are now capable of replacing GaAs/bipolar/BiCMOS circuits in the area of GSM, PCS, IMT-2000, and wireless LAN standards. Though performance of CMOS RF circuits is not superior, rather just comparable to its of bipolar counterpart, but retaining the merits of reasonable cost, high level of integration, and mass productivity, CMOS technologies now prevails in RF domain as well.

The basic architecture of a general RF receiver is shown in Fig.1. The RF signal is detected by the antenna and put through a band pre-select filter. The low noise amplifier (LNA) is the first gain stage of the receiver, and may or may not be tuned to a specific passband. Image reject filtering may be in the signal path before a mixer brings down the RF signal to the intermediate frequency (IF) for further signal processing.

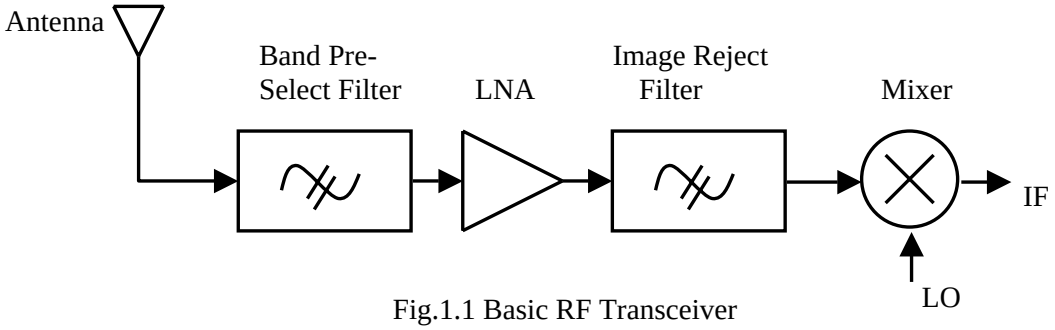

Fig.1.1 Basic RF Transceiver

LNA is the first gain stage in the receiver while contributing as little noise as possible. The LNA impedances should be matched closely to 50 Ω at its input and output for maximum power transfer at radio frequencies because the performance of the filters largely depends on the termination impedance. The output matching condition can be relaxed if the LNA is required to drive an on chip mixer, i.e., the output of LNA goes to the input of a MOSFET. Finally, the LNA must have good reverse isolation so that the local oscillator (LO) signal at the output is not permitted to traverse backwards through the LNA into the antenna.

1.2 Motivation

Design of low power modules for wireless transceivers has been a popular research topic for several years now. One such application that appears to be well suited for RF CMOS design is known as Bluetooth, a short range, 2.4 GHz wireless standard for connecting various communications devices such as mobile phone, wireless headsets, desktop computers and its peripherals. The primary constraint on Bluetooth application is power consumption.

With technology scaling, channel length as well as gate oxide thickness decreases, dictating a decrease in the supply voltage. The increased speed of these smaller devices hold potential for a variety of RF applications in the low GHz range but the decreasing supply voltage will make RF CMOS design even more challenging, especially while striving for low power consumption. To complicate the designer activity, parameters of LNA, e.g., NF, gain, IIP3, power consumption trade with each other.

This work draws its main motivation from these requirements. It tries to provide another step towards a CMOS LNA design for low power application, and reports a new LNA architecture that consumes less power compared to other existing architectures, while providing the same gain, noise figure, CP_{-1dB} and IIP3.

1.3 Organization

This project report is organized as follows. Chapter 2 gives a detailed discussion on noise. It deals with general noise types as well as noise sources present in the MOSFET. The derivation of two port noise parameters and optimum source impedance is also given in this chapter. It also includes the high frequency noise model and the MOSFET two-port noise parameters. Chapter 3 deals with low noise amplifier design. The design issues, various available architectures and device dimensions are given. The proposed new design is also described here. In chapter 4 various simulation results are provided. Chapter 5 provides the conclusion and scope for future work. References are provided at the end of the report. Three appendices are provided. The first explains the BSIM3 noise model. The second lists the procedure about how one measures IIP3 in SPICE. The third appendix provides the BSIM 3.2.4 model used for simulation.

Chapter 2

Noise

2.1 Introduction

Noise plays a very important role in almost all circuit design as it limits the sensitivity of the systems. Noise is generally defined as the "undesired signal". There are many potential sources of noise. They can be external to the system (e.g., atmospheric noise, galactic noise, interference coming from sources like power-line, signal cross-talk, and other electromagnetic waves) or internal to the system. The effect of external noise can be minimized by good shielding mechanism. The internal noise, also referred as fundamental noise, is closely linked to physical phenomena, which characterize the behavior of the circuit components, and hence cannot be reduced by shielding. The noise is mostly due to spontaneous voltage and current fluctuation caused due to random motion of charge carrier.

2.2 Different Types of Noise

Noise can be categorized according to the physical mechanism that generates it. In the following sections different types of noise are discussed briefly:

2.2.1 Thermal Noise

Thermal noise is produced due to random thermal motion of electrons in the conducting media. The thermally agitated charge carriers in a conductor constitute a randomly varying current and thus a randomly varying voltage across a resistor. The thermal noise power spectrum is independent of frequency and it depends only on the absolute temperature [2]. Thermal noise power is given by

$$P_{TH}=kT\Delta f \tag{2.1}$$

Where Δf is the BW over which measurement is done.

The most common sources of thermal noise in RF ICs are resistors and MOS transistors. Purely reactive elements generate no thermal noise.

2.2.2 Shot Noise

The fundamental basis for shot noise (also known as Schottky noise) is the granular nature of the electronic charge. Shot noise occurs only when there is a direct current flowing across a potential barrier. Since charge comes in discrete bundles it implies that there are discontinuous pulses of current every time an electron crosses an energy barrier. Therefore, two conditions are required for shot noise to occur: a flow of direct current and a potential barrier over which the carriers are extracted [2]. Thus linear devices do

not generate shot noise, despite the quantized nature of electronic charge. Shot noise is given by

$$i_n^2 = 2qI_{DC}\Delta f \tag{2.2}$$

Where i_n is the RMS noise current, I_{DC} is the DC current and Δf is the noise BW in Hz.
All nonlinear devices not necessarily exhibit shot noise, e.g., only the DC gate leakage current of FET contributes shot noise and as this gate current is very small, it is an insignificant noise source.

2.2.3 Flicker Noise

At present the origin of the flicker noise is not clearly known. Flicker noise is most prominent in devices that are sensitive to surface phenomena. It is also known as 1 /f noise since its power spectral density is inversely proportional to the frequency. Flicker noise is given by

$$N^2 = \frac{K}{f^n}\Delta f \tag{2.3}$$

Where N is the RMS noise, K is an empirical parameter that is device specific and n is an exponent that is usually close to one.

It is found that a resistor exhibit flicker noise only when there is DC current flowing thorough it, with the noise increasing with the current. In bipolar transistor the flicker noise is entirely due to base current [2].

2.2.4 Popcorn Noise

It is another type of low frequency noise that can be found in integrated circuits but the reason is still not known. It is probably related to the presence of heavy metal ion contamination. Popcorn noise, also known as burst noise, is characterized by a multimodal distribution, that is the noise switches between two or more discrete values at random times [2]. The equation for this noise is given below

$$\mathbf{N}^2 = \frac{K}{1+(f/f_c)^2}\Delta f \tag{2.4}$$

Where K is an empirical, device and fabrication dependent constant and f_c is a corner frequency below which burst noise density flattens out.

2.3 Noise in MOSFET

The MOS transistors are the main source of noise in RF ICs. Different types of noise in a MOSFET and their origins are discussed below.

2.3.1 Drain current Noise

For a MOSFET in normal operation, a resistive channel exists between the drain and the source. The drain current noise is given by the following expression

$$i_{nd}^2 = 4kT\gamma g_{d0}\Delta f \tag{2.5}$$

Where g_{d0} is the drain-source conductance at $V_{DS}=0$.

For long channel devices $\gamma=1$ at zero V_{DS} and approaches 2/3 in saturation. For the case of short channel devices γ may be as high as 2-3, depending on the bias condition. Since the origin of this excess noise is carrier heating by the large electric fields it is important to use minimum practical drain voltage [2].

2.3.2 Gate Noise

The fluctuating channel potential couples through gate-channel capacitance into the gate terminal and generate noisy gate current, which is frequency dependent. This noise becomes much significant in radio frequency [2]. Gate noise can be expressed as

$$\mathbf{i}_{ng}^2 = 4kT\delta g_g \Delta f \tag{2.6}$$

Where the parameter $g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}$ and δ is the gate noise coefficient having a value of 4/3 for long channel devices.

2.3.3 Flicker Noise

Since MOSFETs are surface devices, they exhibit more flicker noise than bipolar devices. Larger MOSFETs exhibit less 1/f noise because large gate capacitance smoothens the fluctuation in channel charge [2]. Drain noise current due to flicker noise is given by

$$\mathbf{i}_n^2 = \frac{K}{f}\frac{g_m^2}{WLC_{ox}^2}\Delta f \tag{2.7}$$

Where K is a device specific constant. Thus for a fixed transconductance, larger gate area and thinner dielectric reduces flicker noise.

2.3.4 Other Noise sources

In addition to the noise sources that are described above, MOSFET have other sources of noise also which generally do not contribute significant noise. They are listed below [14]

a) Thermal noise associated with distributed substrate resistance R_G. This noise is coupled to the drain current through substrate transconductance g_{mb}.

b) Thermal noise associated with distributed gate resistance R_G.The contribution of this noise can be reduced by interdigitating the device.
c) Thermal noise associated with the terminal source resistance (R_S) and the terminal drain resistance (R_D).
d) Noise generated in the impact ionization process. The amount of noise is proportional to the current flowing thorough the substrate.

2.4 Noise Parameters

This section describes how a noisy two port can be modeled by four noise parameters and from these parameters how one can derive the condition for optimum noise performance.

2.4.1 Noise Factor

Noise factor is defined as

$$F=\frac{\text{Total output noise power}}{\text{Output noise due to input source}}. \tag{2.8}$$

The noise factor measures how much a system degrades the signal to noise ratio when any signal goes through it.

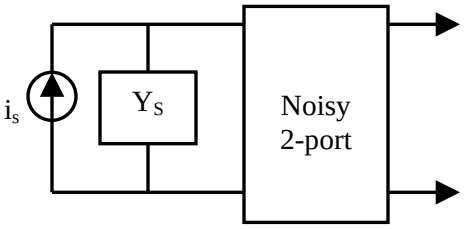

Fig.2.1 Noisy 2-port driven by noisy source

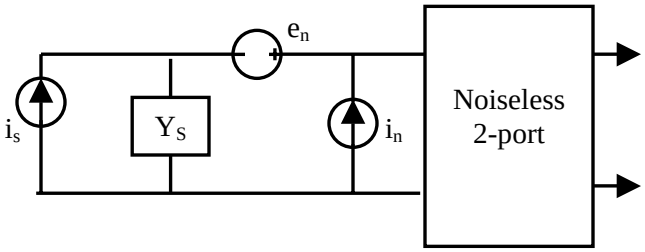

Fig.2.2 Equivalent noise model

Fig.2.1 shows a two port driven by a source that has an admittance Y_S and an equivalent noise current i_s. In Fig.2.2 all noise appears as inputs to the noiseless network so that calculation of noise factor becomes easier. One needs to compute the ratio between total short circuit mean square noise current and short circuit mean square noise current due to input sources. Assuming that the noise powers of the source and two ports are uncorrelated, the expression of noise figure becomes

$$F=\frac{i_s^2+|i_n+Y_s e_n|^2}{i_s^2} \tag{2.9}$$

To find the correlation between e_n and i_n, i_n is expressed as the sum of two components

$$i_n= i_c+ i_u \tag{2.10}$$

Here i_c is correlated with e_n and may be taken as proportional to e_n, with the proportionality constant being the *correlation admittance (Y_c).*

$$i_c = Y_c\, e_n \tag{2.11}$$

Using equation 2.9, 2.10, 2.11, the noise factor becomes

$$F=\frac{i_s^2+|i_u+(Y_c+Y_s)e_n|^2}{i_s^2} =1+ \frac{i_u^2+|Y_c+Y_s|^2 e_n^2}{i_s^2} \tag{2.12}$$

The expression of 2.12 contains three independent noise sources, each of which may be treated as thermal noise produced by an equivalent resistance or conductance.

$$R_n=\frac{e_n^2}{4KT\Delta f} \tag{2.13}$$

$$G_u=\frac{i_u^2}{4KT\Delta f} \tag{2.14}$$

$$G_s=\frac{i_s^2}{4KT\Delta f} \tag{2.15}$$

Finally the expression for noise factor becomes

$$F=1+\frac{G_u+[(G_c+G_s)^2+(B_c+B_s)^2]R_n}{G_s} \tag{2.16}$$

In expression 2.16 all the admittance are expressed as sum of conductance and susceptance.

2.4.2 Optimum source admittance

The final expression of noise factor gives the general conditions for minimizing noise factor. Taking the derivative of equation 2.16 with respect to source admittance and equaling it to zero gives

$$B_s = -B_c = B_{opt} \tag{2.17}$$

$$G_s =\sqrt{\left(\frac{G_u}{R_n} + G_c^2\right)} = G_{opt} \tag{2.18}$$

Using these expressions of optimum source admittance, minimum noise factor becomes

$$F_{min}=1+2R_n[G_{opt}+G_c] = 1+2R_n[\sqrt{(\frac{G_u}{R_n} + G_c^2)}+G_c] \quad (2.19)$$

The noise factor in terms of F_{min} and the source admittance becomes

$$F= F_{min}+\frac{R_n}{G_s}[(G_s-G_{opt})^2+(B_s-B_{opt})^2] \quad (2.20)$$

2.4.3 Drawbacks of classical noise optimization

The above noise optimization technique has some inherent limitations as listed below

a) No specific guidelines about device size that will minimize noise.
b) Power consumption is not considered.

2.5 High frequency MOSFET noise model

The standard CMOS noise model is shown in Fig.2.3. Channel thermal noise (i_{nd}^2 as given in equation 2.5) which is dominant noise source in CMOS devices, is modeled as a shunt current source in the output circuit of the device.

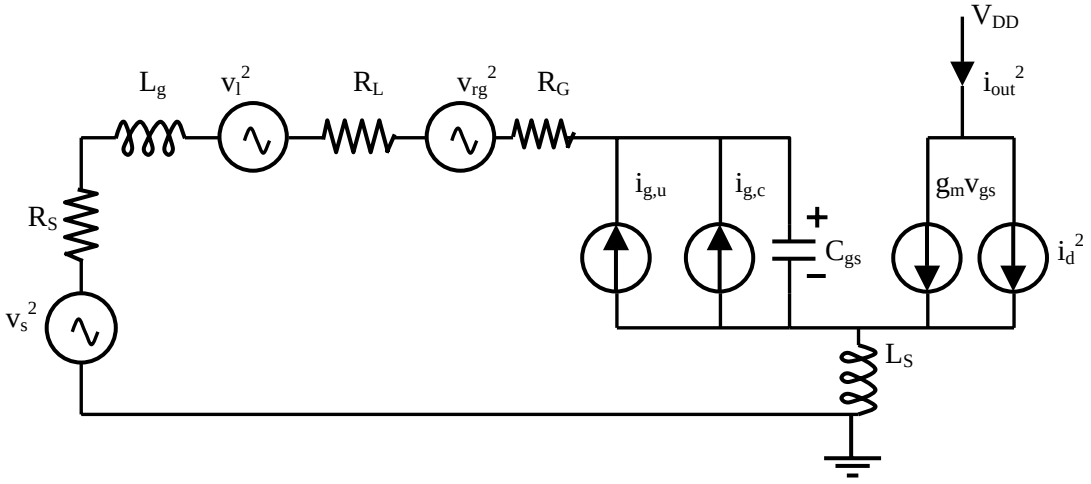

Fig.2.3 High Frequency MOSFET noise model

A resistance in series with gate and an accompanying noise generator models the noise source due to distributed gate resistance [1]. For calculation of noise the distributed gate resistance is given by

$$R_g=\frac{R_{SH}W}{3n^2L} \quad (2.21)$$

Where R_{SH} is the sheet resistance of the polysilicon (W/L) is the aspect ratio of the device and n is the number of gate fingers used to lay out the device. Interdigitation or reducing sheet resistance can minimize the contribution of this noise.

At very high frequency, approaching ω_T, the gate impedance of the device produce significant phase shift from its purely capacitive nature. This phase shift as well as the gate noise explained in Section 2.3.2 can be modeled by adding a real, noiseless conductance (g_g) in the gate circuit and a shunt noise current i_g^2 as shown in Fig.2.4.Thevenin's representation of the gate noise model is presented in Fig.2.5 where

$$v_g^2 = 4kT\delta r_g \tag{2.21}$$

$$\text{and } r_g = \frac{1}{5g_{d0}} \tag{2.22}$$

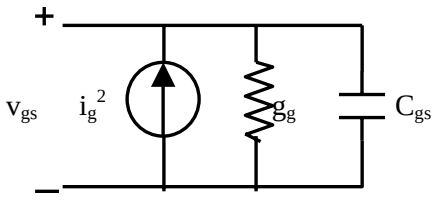

Fig.2.4 Gate circuit model for induced noise

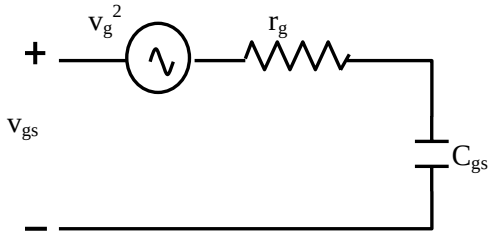

Fig.2.5 Thevenin's representation

The above figures are interchangeable for frequencies where

$$\omega << \frac{5g_{d0}}{C_{gs}} = \frac{5\omega_T}{\alpha} \tag{2.23}$$

The gate noise is partially correlated with the drain noise and the correlation coefficient is given by

$$c = \frac{i_g i_d}{\sqrt{i_g^2 i_d^2}} \approx 0.395j \tag{2.24}$$

This correlation can be treated by modeling gate noise as sum of two current sources, one that is fully correlated with drain noise and the second one being uncorrelated with the drain noise [1]. So the gate noise can be expressed as

$$\frac{i_g^2}{\Delta f} = 4kT\delta g_g(1-|c|^2) + 4kT\delta g_g|c|^2 \qquad (2.25)$$

Uncorrelated correlated

2.6 MOSFET two-port noise parameter

MOSFET noise model consists of two sources: drain current noise (i_{nd}^2) and gate current noise (i_{ng}^2). To derive the two-port noise parameters, which characterize the internal noise of the device, these two fundamental MOSFET noise sources are reflected back to the input pair as a different pair of equivalent input generators (one voltage and one current source) [2]. Table 1.1 listed the MOSFET two-port noise parameters.

Table 1.1: MOSFET two-port noise parameters

Parameter	Expression
G_c	~ 0
B_c	$\omega C_{gs}(1+\alpha\|c\|\sqrt{\frac{\delta}{5\gamma}})$
R_n	$\frac{\gamma g_{d0}}{g_m^2} = \frac{\gamma}{\alpha}\cdot\frac{1}{g_m}$
G_u	$\frac{\delta\omega^2 C_{gs}^2(1-\|c\|^2)}{5g_{d0}}$

Where $\alpha = g_m/ g_{d0,}$ is unity for long channel devices and gradually decreases with shrinking channel length.

With these parameters the optimum source impedance and the corresponding noise figure can be determined. It comes out that minimum noise figure is given by

$$F_{min} \simeq 1+ \frac{2}{\sqrt{5}}\frac{\omega}{\omega_T}\sqrt{(\gamma\delta(1-|c|^2)} \qquad (2.26)$$

Two observations can be made from the above equation. Firstly if no gate current noise i.e., if δ=0, the minimum noise figure is 0dB.This impossible result tells that gate noise must exist. Secondly the improvements in ω_T that occurs with technology scaling also improve noise figure at any given frequency[2].With source admittance other than optimum values, noise factor can be expressed as

$$F = F_{min} + \frac{R_n}{G_s}\left[(G_s - G_{opt})^2 + (B_s - B_{opt})^2\right] \quad (2.27)$$

Where $$B_{opt} = -B_c = -\omega C_{gs}\left(1 + \alpha|c|\sqrt{\frac{\delta}{5\gamma}}\right) \quad (2.28)$$

And $$G_{opt} = \sqrt{\left(\frac{G_u}{R_n} + G_c^2\right)} = \alpha\omega C_{gs}\sqrt{\left(\frac{\delta}{5\gamma}(1 - |c|^2\right)} \quad (2.29)$$

Chapter 3

LNA Design

3.1 Introduction

Low Noise Amplifiers (LNA) are the backbone of radio frequency (RF) communications receivers. In addition to providing gain while adding the minimum possible noise, the additional constraint of LNA design arise from the fact that it should allow a large signal without distortion and present a matching impedance to the input source. This chapter discusses the issues related to the design of a low noise amplifier. It also describes various LNA circuit architectures, and the new architecture proposed in this thesis.

3.2 Input impedance match

The input impedance of MOSFET is capacitive in nature so providing a proper match to 50-Ω source is difficult without degradation of noise figure. Some approaches that are used to achieve this goal are discussed below:

3.2.1 Common source amplifier with shunt input resistor

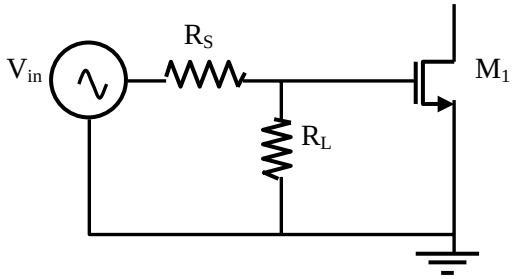

Fig.3.1 CS amplifier with shunt input resistor

Noise factor of the above circuit is calculated as follows [10]

- Noise of source: $4KTR_S$
- Noise of the shunt resistor: $4KTR_L$
- If $R_S=R_L$, input circuit acts as voltage divider, noise voltage of R_S and R_L is halved and the power becomes one-fourth.
- Output Noise due to source: $4KTR_SG_a$.
- Total noise at output = $4KTR_SG_a+ P_{ni}$

$$\text{Noise Factor} = \frac{\text{Total Output Noise}}{\text{Output noise due to source}}$$

$$= \frac{KTR_SG_a + KTR_SG_a + P_{ni}}{KTR_SG_a}$$

$$= 2 + \frac{P_{ni}}{KTRG_a} \quad [\text{with } R_S = R_L = R]$$

$$= 2 + \frac{V_{ni}^2}{KTRA_v^2}$$

$$= 2 + 4\frac{\gamma}{\alpha}\frac{1}{g_{m.}R} \; ** \qquad (3.1)$$

** Putting $V_{ni}^2 = 4kT\gamma g_{d0}R^2$, mean square drain noise voltage; $A_v = (g_mR)$; and substituting $\alpha = g_m / g_{d0}$.

The minimum NF, given in the above equation, is achieved assuming operation to be in low frequency range and ignoring gate current noise. So the NF increases when either of these two assumptions is no more valid.

3.2.2 Shunt–Series Amplifier

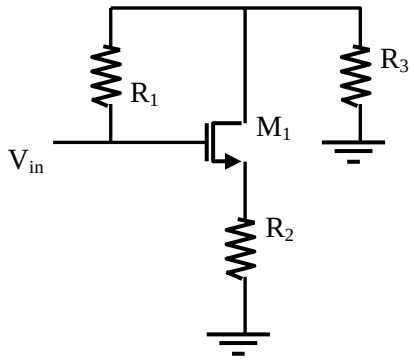

Fig.3.2 Shunt Series Amplifier

This circuit provides broadband real input impedance. And though it does not attenuate the signal before amplifying, yet the resistive feedback continues to generate thermal noise. Moreover it cannot present to the transistor the optimum impedance over a wideband. This configuration is frequently used in many LNA applications.[2]

3.2.3 Common Gate Configuration

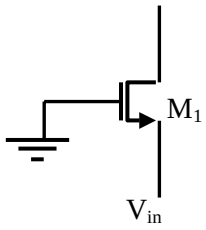

Fig.3.3 Common Gate amplifier

This is another method to achieve resistive input impedance. Since the resistance looking into the source terminal is $1/g_m$, a proper selection of device size and bias current can provide the desired input impedance [2]. Assuming low frequency operation and no gate noise, the lower bound of the NF of this amplifier is given by

$$F = 1 + \frac{P_{ni}}{4KTR_S G_a}$$

$$= \frac{4kT\gamma g_{d0} R^2}{4KT\frac{1}{g_m} g_m^2 R^2}$$

$$= 1 + \frac{\gamma}{\alpha} \qquad (3.2)$$

3.2.4 Lee's Architecture: Inductive Degeneration

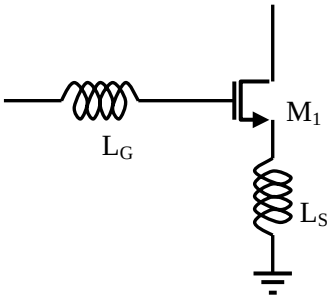

Fig.3.4 CS amplifier with inductive degeneration

This circuit is able to generate resistive impedance using reactive components only, which implies no addition of extra thermal noise of resistor and no attenuation at the input. This architecture is the most commonly used input stage of LNA.

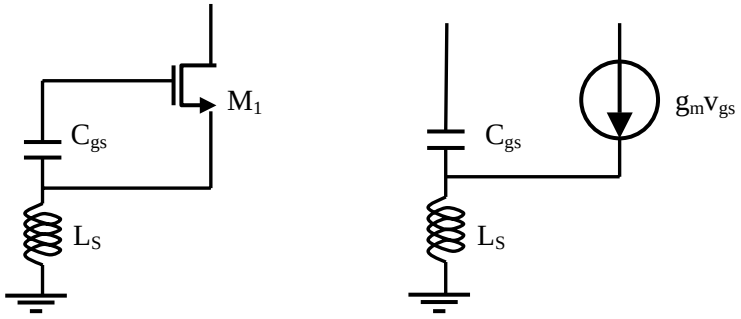

Fig.3.5 Generation of resistive component without Resistor

The idea here is, generate a current proportional to 1/s and push it into impedance that varies with s, will have the effect of real impedance [10].

$$\text{Current through } L_S,\quad I_L = I_{in}+g_m(V_g-V_s)$$
$$= I_{in}+g_m\left(\frac{I_{in}}{sC_{gs}}\right) \tag{3.3}$$

$$\text{Voltage across } L_S, V_L = sL_sI_L$$
$$= sL_s\left(I_{in}+g_m\left(\frac{I_{in}}{sC_{gs}}\right)\right)$$
$$= I_{in}\left(sL_s+\frac{g_mL_s}{C_{gs}}\right) \tag{3.4}$$
$$= I_{in}(\text{Inductor+Resistor})$$

$$\text{Therefore, Resistor added, } R_{in} = g_m\left(\frac{L_s}{C_{gs}}\right) \tag{3.5}$$

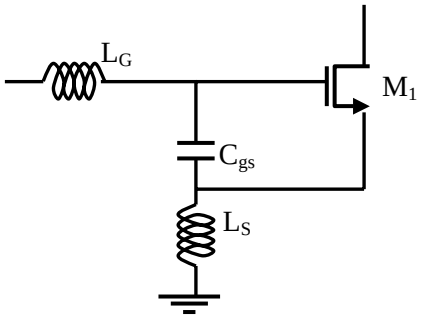

Fig.3.6 Setting the impedance and resonance frequency independently

The circuit in Fig.3.6 with a single inductor (L_S) resonates at $\omega_0 = \frac{1}{\sqrt{L_sC_{gs}}}$ and provides a resistive input impedance given by equation 3.5.As both ω_0 and R_{in} are dependent on L_s, therefore to allow independent setting of these two parameters the

inductor is splitted on two halves. The input resistance remains $R_{in} = g_m \frac{L_s}{C_{gs}}$ but the center frequency becomes

$$\omega_0 = \frac{1}{\sqrt{(L_s+Lg)C_{gs}}} \tag{3.6}$$

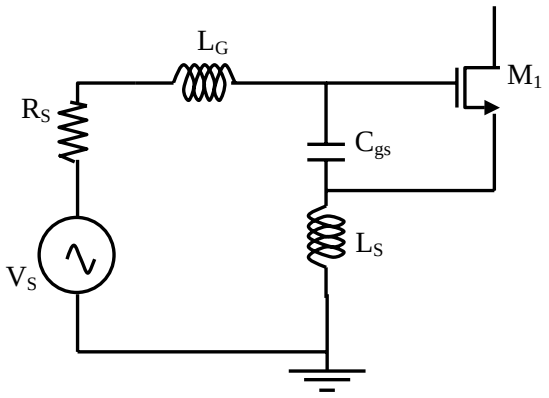

Fig.3.7 Finding transconductance of Lee's Architecture

The total transconductance of the input stage at resonant condition is

$$Gm = g_m Q_{in} = g_m \frac{\sqrt{\frac{L_s+L_g}{C_{gs}}}}{R_s+g_m\frac{L_g}{C_{gs}}} \tag{3.7}$$

Substituting $\omega_t = \frac{g_m}{C_{gs}}$ and $\omega_0 = \frac{1}{\sqrt{(L_s+Lg)C_{gs}}}$

$$G_m = \frac{\omega_t}{2\omega_0 R_s} \tag{3.8}$$

So the overall transconductance is independent of the device transconductance.

3.3 Noise optimization technique

If one choose gate width of the amplifier MOSFET from the expression of G_{opt} given in equation 2.27, in which G_{opt} is a function of gate capacitance then though the corresponding NF is very close to F_{min} but the power consumed would be unacceptably

high. So some optimization method is required to find the optimum device dimension that minimizes noise, once a specified bound on power consumption is given [2].

Detailed derivation gives the width of the optimum device as

$$W_{opt} = \frac{3}{2} \frac{1}{\omega L C_{ox} R_s Q_s} \tag{3.9}$$

The value of $Q_s (= \frac{1}{\omega C_{gs} R_S})$ that leads to the power- constrained minimum noise figure is

$$Q_{sp} = |c| \sqrt{\frac{5\gamma}{\delta}} \left[1 + \sqrt{\left(1 + \frac{3}{|c|^2}\left(1 + \frac{\delta}{5\gamma}\right)\right)}\right] \cong 4 \tag{3.10}$$

The achievable noise figure is relatively insensitive to values of Q_{sp} between 3.5 and 5.5, changing by 0.1 dB or less over this range.
With a device of width W_{opt}, the noise figure obtained within the power constraintis

$$F_{min,P} \cong 1 + 2.4 \frac{\gamma}{\alpha} \frac{\omega}{\omega_T} \tag{3.11}$$

With $\alpha = \frac{g_m}{g_{d0}}$.

This noise optimization technique is quite attractive as it balances all parameters of interest. Since both effective transconductance and noise figure involves ω_T, both improve simultaneously as ω_T increases [2].

3.4 Architectures

After the input stage is designed, the amplifying and the output stage of the LNA is decided depending upon the application, i.e., whether low power or wide bandwidth is necessary. Basic LNA architecture along with two advanced topologies are discussed below. Both the augmented topologies try to reduce power consumption by reducing supply voltage or drain current.

3.4.1 Basic LNA circuit

Fig.3.8 shows a basic single-ended LNA circuit. Due to the inherent shielding effect of the cascoding transistor M_2, input transistor is not affected by the voltage variation at the output. The total node capacitance at the drain of M_2 resonates with inductance L_d to increase gain at center frequency because gain of the cascode stage is proportional to the drain resistance at M_2 and at resonant frequency the equivalent impedance of a LC tank circuit is very high.[2]

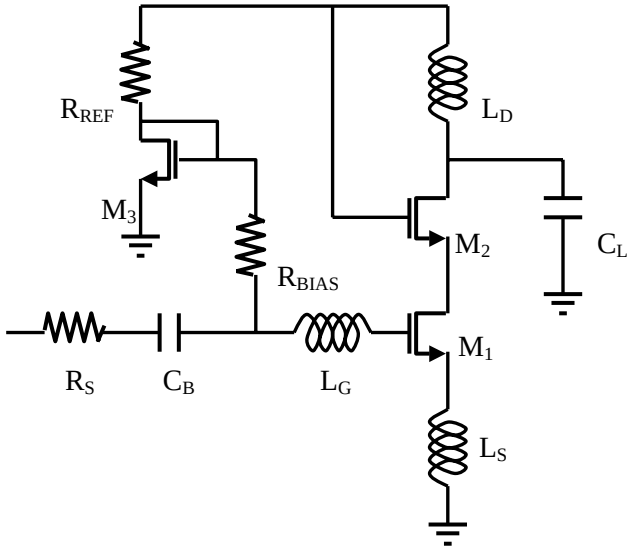

Fig.3.8 Basic Single ended LNA with current–mirror biasing

M_3 forms a current mirror with M_1.The resistor R_{bias} is chosen large enough such that its equivalent noise current ($i_n^2=\frac{4KTf}{R}$) can be ignored [2]. DC blocking capacitor is added to prevent gate-to-source bias of $M_1$from being changed spuriously. The value of C_B is chosen to have negligible reactance at signal frequency.

3.4.2 Folded Cascode structure

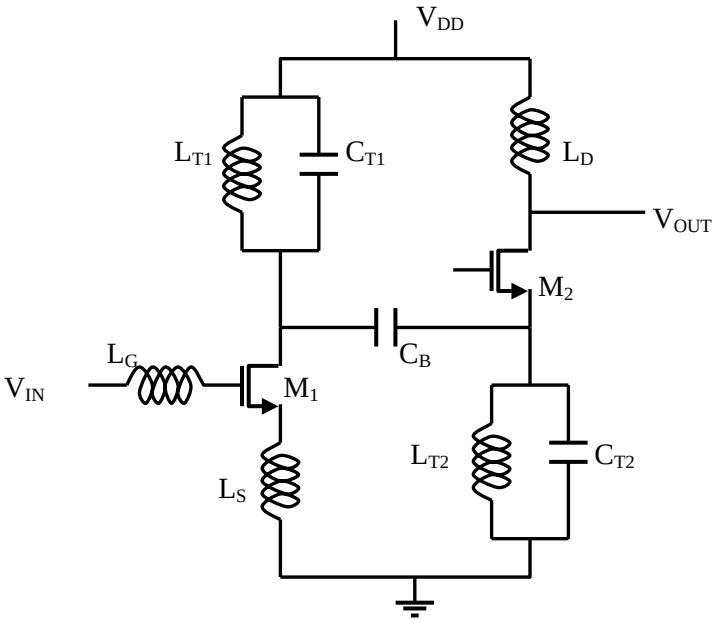

Fig.3.9 Folded Cascode LNA

In the cascode LNA there are two MOSFETs in series so if the threshold voltage is V_T**,** the V_{DD} should be at least $2V_T$**.** The above figure shows a folded cascode structure to lower the supply voltage. At DC, the inductor, L_{t1} and L_{t2} provides a low resistance path

to bias both the MOSFETs individually. If the threshold voltage is V_T, the V_{DD} only needs V_T to drive the MOSFET.At RF, the LC-tanks have high impedances at resonance, so it is almost open for RF signal and RF signal flows from the M_1 through C_p to the source of M_2 [9].

The operation of LC-tank is limited by the quality factor of the LC-tank circuit. Fig.3.10 (a) shows a LC-tank model with a parasitic resistance R_S. Small amount of current will be lost by LC-tank because of the parasitic resistance (R_S.) of the on-chip spiral inductor [9]. The quality factor of the LC-tank is defined as:

$$Q=\frac{\omega L_s}{R_s} \tag{3.9}$$

The equivalent parallel circuit is as shown 3.10.(b) where

$$R_p= (1+Q^2)R_s \tag{3.10}$$

$$L_p= \cdot\frac{1+Q^2}{Q^2} L_s \tag{3.11}$$

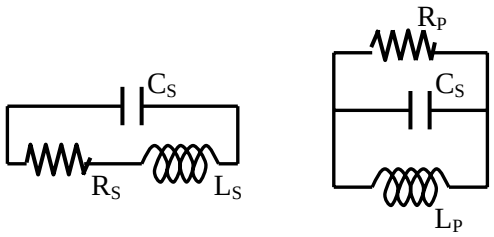

Fig.3.10 LC tank and its Equivalent model

There are some current lost from the two LC-tanks and a losing factor is defined to calculate the lossy current as:

$$\eta = \frac{i_{Loss}}{i_d} = \frac{\frac{1}{g_{m2}}}{R_p||R_p+\frac{1}{g_{m2}}} = \frac{\frac{1}{g_{m2}}}{\frac{R_p}{2}+\frac{1}{g_{m2}}} \tag{3.12}$$

Where i_d is the current flowing at the drain of the common source transistorM_1 and i_{Loss} is the part of the current flowing through $R_{p1}$and R_{p2}.(Here it is assumed $R_{p1}= R_{p2}= R_p$ and R_m= Input resistance of Cascoding transistor = $1/g_{m2}$).

3.4.3 Current Reuse method

The goal of this method is to achieve g_m and ω_T of a single device with less current. Fig.3.11 (a) shows a single NMOS device that has aspect ratio W/L with drain current I_D. Fig.3.11 (b) shows two NMOS device in parallel, each having aspect ratio (1/2)(W/L) and drain current (1/2)I_D. Thus the transconductance of the compound device is same as that of fig.3.11 (a). The total transconductance in fig.3.11(c) is $g_{mt}=g_{mp}+g_{mn}$. Since the mobility of the PMOS device is lower, g_{mt} will be lower than g_m, e.g. if $\mu_p \cong 0.5\mu_n=$, then $g_{mt}\cong 0.85g_m$. This reduction in g_{mt} results an increase of 0.2 dB in NF but this is tolerable because the drain current is halved [3].

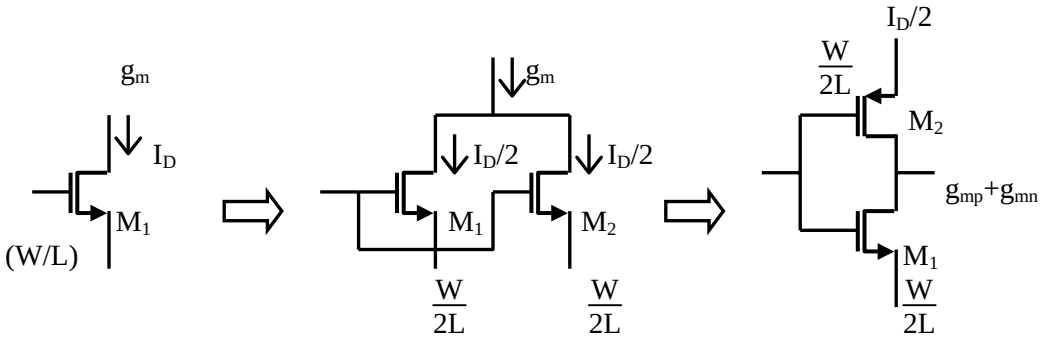

Fig 3.11 Equivalence between p-n input stage and classic NMOS input stage

3.5. Proposed LNA architecture

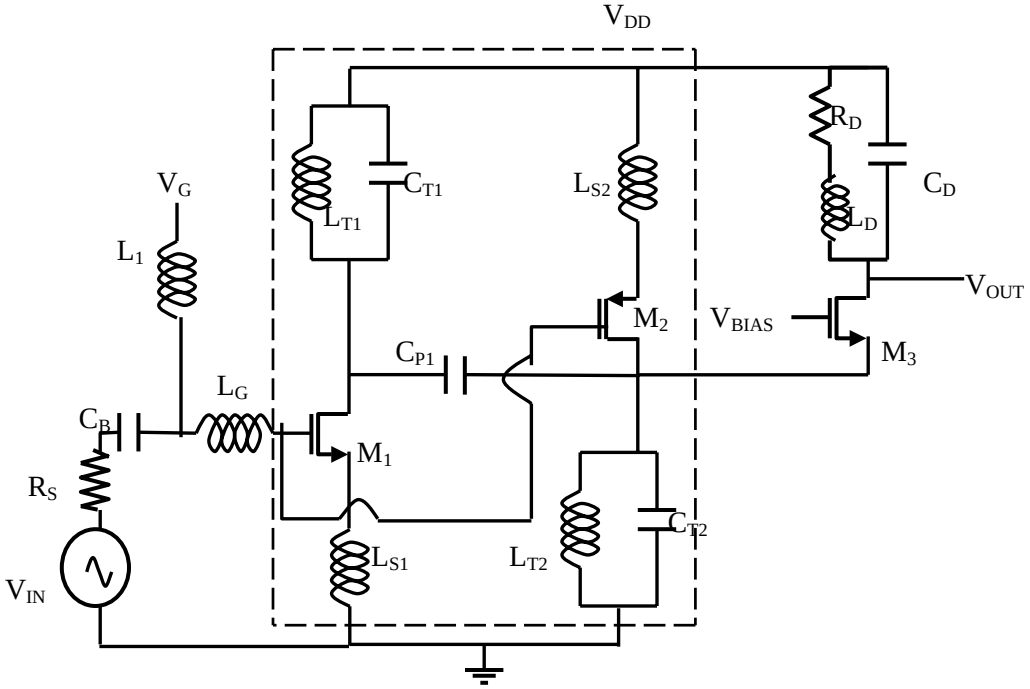

Fig.3.12 Complete schematic of proposed LNA architecture

Fig.3.12 shows the newly proposed design of the LNA. The part of the circuit in dotted line is the modified inverter. At DC, M_1 and M_2 are isolated by the capacitor C_{P1}. They are individually biased by V_{DD} through the inductors connected at their source and drain (L_{S1}, L_{T1}, L_{S2}, L_{T2}). But at the operating frequency the LC tank circuits act as open circuit and the coupling capacitor becomes short circuit and the circuit inside the dotted line becomes an inverter.

3.5.1 Small signal analysis

The small signal equivalent circuit of the first stage of the proposed architecture is shown below. It is assumed that the tuned circuits are open and coupling capacitor has negligible reactance at resonance frequency.

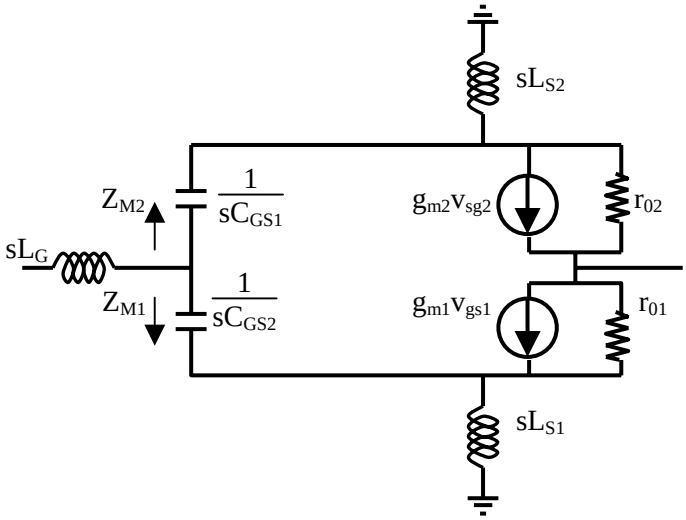

Fig.3.13 Small signal equivalent of inverter

The input impedance of the above circuit is given by

$$Z_{in}=sL_G + (Z_{M1}||Z_{M2}) \tag{3.13}$$

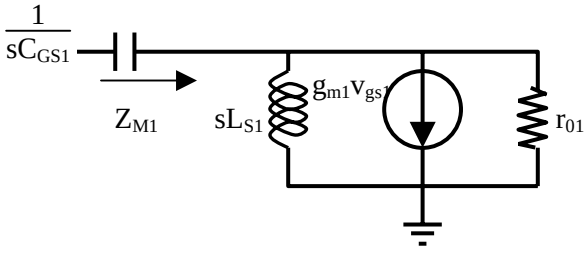

Fig.3.14 Derivation of Z_{M1}

$$Z_{M1}=\frac{v_g}{I_{in}}=\frac{v_g}{(v_g-v_{s1})sC_{GS1}}=\frac{1}{sC_{GS1}}+sL_{S1}+g_m\frac{L_{S1}}{C_{GS1}} \quad (3.14)$$

$$Z_{M2}=\frac{v_g}{I_{in}}=\frac{v_g}{(v_g-v_{s2})sC_{GS2}}=\frac{1}{sC_{GS2}}+sL_{S2}+g_m\frac{L_{S2}}{C_{GS2}} \quad (3.15)$$

Assuming $C_{GS1}=C_{GS2}=C_{GS}$, $L_{S1}=L_{S2}=L_S$

$$Z_{in}=sL_G+\frac{1}{2}\left[\frac{1}{sC_{GS}}+sL_S+g_m\frac{L_S}{C_{GS}}\right] \quad (3.16)$$

$$=\left(sL_G+\frac{1}{2}sL_S+\frac{1}{2}\frac{1}{sC_{GS}}\right)+\frac{1}{2}g_m\frac{L_S}{C_{GS}} \quad (3.17)$$

From the expression of 3.17 the resonance and matching condition are found to be

$$\omega_0=\frac{1}{\sqrt{C_{GS}(2L_G+L_{S1})}} \quad (3.18)$$

$$\omega_{T1}L_{S1}=2R_S\ ,\ \omega_TL_{S2}=2R_S \quad (3.19)$$

Thus the input impedance of the circuit at resonance is resistive given by $\frac{1}{2}g_m\frac{L_S}{C_{GS}}$.

The overall transconductance of a traditional inverter is $g_{mp}+g_{mn}$, where g_{mp} and g_{mn} are the individual transconductance of the PMOS and NMOS transistor. At resonance the gate to source voltage is Q times as large as the input voltage [2]. The overall transconductance is given by

$$G_m=(g_{mp}+g_{mn})Q \quad (3.20)$$

Where $Q=\frac{1}{\omega_0C_{GS}R_S}$ and $R_S=\frac{1}{2}g_m\frac{L_S}{C_{GS}}$.

So the voltage gain of the first stage is $A_{V1}=G_mZ_1$, where $Z_1$is the load impedance and as the inverter stage is followed by a common gate stage, $Z_1=\frac{Z_L}{g_mr_0}$, input impedance of a common gate stage with load Z_L.

The voltage gain of a common gate stage with load Z_L is also given by $A_{V2}=g_mZ_L$.So the overall gain on the proposed amplifier becomes

$$A_{TOTAL}=A_{V1}.A_{V2}=\frac{G_mZ_L^{\,2}}{r_0} \quad (3.21)$$

3.5.1 Design parameters of LNA

The widths of PMOS and NMOS of the inverter circuit are calculated as follows

$$W_{OPT} = \frac{1}{3\omega_0 L C_{ox} R_S} = 285\mu m \tag{3.22}$$

Where $\omega_0 = 2\pi * 2.4 * 10^9$, L=0.18μm, C_{OX} = 0.294pF, $R_S = 50\Omega$

$$C_{OX} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} = 8.62 pF/\mu m^2 \tag{3.23}$$

Where ε_r= relative permittivity of SiO_2 =3.9, $\varepsilon_0 = \frac{1}{36\pi * 10^9}$ F/m; t_{ox}=oxide thickness = 4 nm.
In the inverter circuit width is taken as half of optimum width, $W_1 = W_2 = 285/2 \cong 143\mu m$.

The value of L_G, L_{S1} and L_{S2} are calculated from the equations

L_G=6.82nH; L_{S1}=1.32nH; L_{S2}=1.55nH;
Since $\mu_n > \mu_p \Rightarrow \omega_{Tn} > \omega_{Tp} \Rightarrow L_{S1} < L_{S2}$

The values of the components of the tuning circuits are chosen to resonate at 2.4GHz.

$L_{t1} = L_{t2}$=2.2nH
$C_{t1} = C_{t2}$=1.7pF

The tuning load at the output also resonates at the same frequency and their values are given below:

L_D= 3.0nH
C_D=1.4pF

3.5.2 Bias Circuit

V_G is set at half of V_{DD} so that V_{GS} of both M_1 and M_2 are equal. The value of L_1 is chosen to give high impedance at operating frequency and thus prevents the AC signal from going to ground. The bias circuit providing V_G and V_{BIAS} is shown in Fig.3.13. Bias voltage is taken from point A, whose value is determined by R_1 and width of M_5. The required bias voltage at point A determines overdrive voltage (V_{GS}-V_{TH}) of M_5. So the size of M_5 is kept to small value, which implies small drain current and thus minimizing the power overhead.

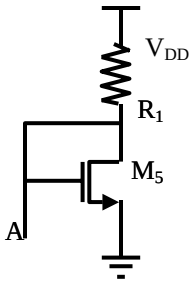

Fig.3.15 Bias circuit of LNA

As the drains of M_1 and M_2 are separated in DC condition, voltages at these points are well defined. So this architecture stabilizes the biasing point of inverter.

3.5.3 Output stage

The output of the inverter is fed to a CG amplifier that has a tuned LC circuit at its drain. The LC tank resonates at operating frequency and gives a very high gain. A small resistor (R_D) is added in series with L_D to provide the required bandwidth.

The output of LNA is kept open circuit because in an integrated RF transceiver output of LNA goes to input of the mixer, so the output load will be a capacitive. But if the LNA is to be tested independently or the input impedance of the mixer is resistive with low value (e.g. 50 Ω) then a buffer is required to lower the output impedance of LNA. The voltage gain of buffer is given by

$$A_{v,\,buffer} = \frac{R_L}{R_L + 1/g_m}. \tag{3.24}$$

From the above equation it is observed that to match a 50Ω load a very high g_m is needed which implies large current and thus increased power consumption. Due to these reasons no buffer is added in the output circuit of the proposed LNA.

Chapter 4

Simulation Results

4.1 Introduction

The simulations of the proposed architectures as well as for degenerated current reuse LNA and folded cascode LNA were done using ibm-7sf/t4az MOSIS 0.18μm SPICE Level 8 parameters in 2.4 GHz. In an RF receiver the output of the LNA goes to the input of a mixer so the LNA will have a capacitive load, which will resonate with the output tank circuit of LNA. So all the parameters of the LNA have been taken under open circuit conditions, i.e., without any termination.

4.2 Results and discussion

The following sub-sections describe in detail the performance of the proposed architecture in terms of gain, noise figure, -1 dB compression point and IIP3. Sensitivity analysis is also carried on the proposed LNA. The last section compares the performances of different LNAs.

4.2.1 Gain and Noise Figure

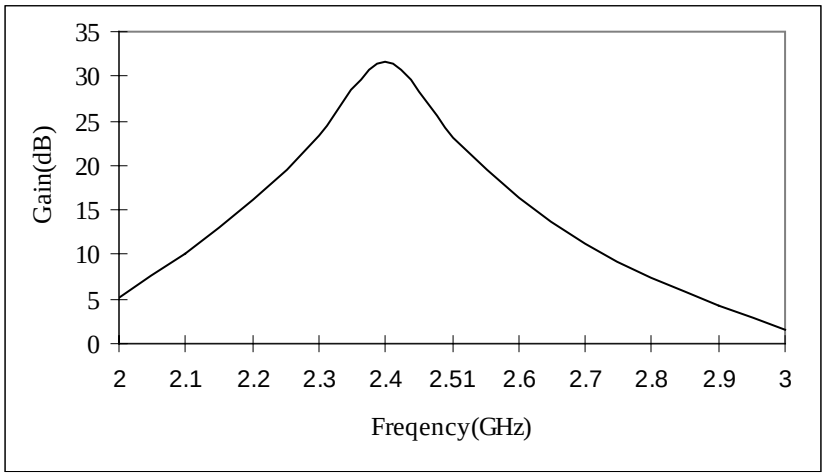

Fig.4.1 Frequency response of proposed LNA

Fig.4.1 shows the AC frequency response of the proposed LNA. As the LNA uses Lee's architecture in the input side and LC tuned load in the output of amplifier, it has a bandpass characteristic. There exists a trade off between the bandwidth (BW) of the LNA and its gain. The LNA bandwidth needed in a 2.4 GHz RF system is around 80 MHz.

Therefore, in the output LC tank circuit a small resistor is added to achieve the required BW whereas all the other inductors are taken as ideal.

The variation of noise figure with frequency is shown in Fig.4.2.

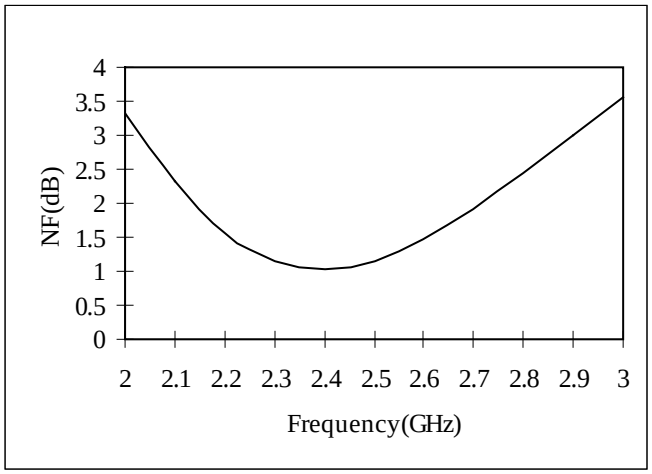

Fig.4.2. Noise figure vs. Frequency

The variation of NF and gain with change in supply voltage is given in Fig.4.3. As explained in the section 3.5, V_G is kept at $V_{DD}/2$, so with increasing V_{DD} overdrive voltage (V_{GS}-V_{TH}) of M_1 and M_2 also increases, thereby increasing drain current as well as transconductance (g_m). This increase in g_m increases gain of the circuit ($A_V=g_mZ_L$).

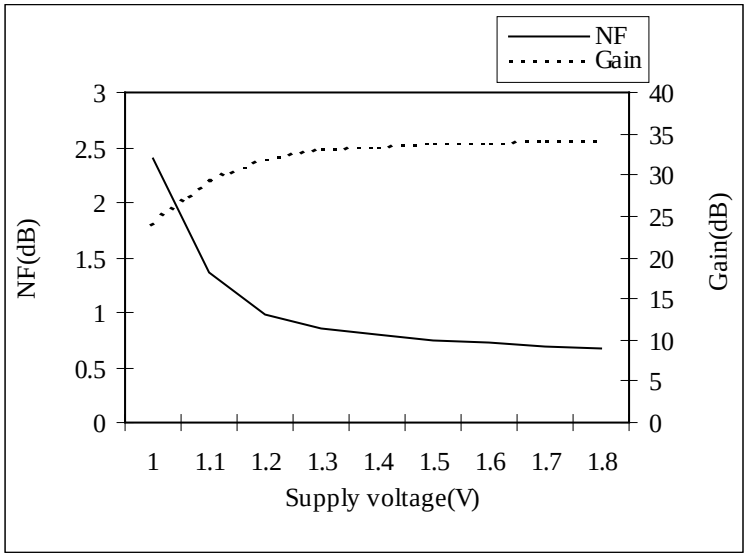

Fig.4.3. Gain and NF vs. Supply voltage

The decrease in noise figure with V_{DD} is explained as follows:

$$NF=\frac{S_i/N_i}{S_0/N_0}=\frac{N_0}{A_vN_i}=\frac{AvN_i+N_{int}}{A_vN_i}=1+\frac{N_{int}}{A_vN_i} \quad (4.1)$$

Where Av=gain of the circuit, N_{int} = internal noise of the circuit, S_i/N_i = input SNR, S_0/N_0=output SNR.
From equation 4.1 it is observed that if A_V increases then noise factor decreases as shown in Fig.4.3.

4.2.2 Linearity

A two-tone IIP3 test was carried in each case using frequencies 2.4 GHz and 2.41 GHz. The 3rd order intermodulation frequencies are 2.39 GHz and 2.41 GHz. The procedure of measuring IIP3 in SPICE is given in Appendix B. Generally IIP3 is measured by increasing input power and observing its relationship with output power. But as already explained in section 3.5 there is no termination resistor at the output load of the proposed LNA circuit. Therefore it is not possible to measure the output power as power is given by V^2/R. If one measures IIP3 using equation 4.1 then one need not worry about the termination resistor or output power.
The expression for measuring IIPn is given by [12]

$$IIPn=A+\frac{\Delta}{n-1} \quad (4.2)$$

Where IIPn = n^{th} order input intercept point (dBm)
A = input signal level (dBm)
Δ = Difference between desired signal and undesired distortion (dB)
n = order of distortion

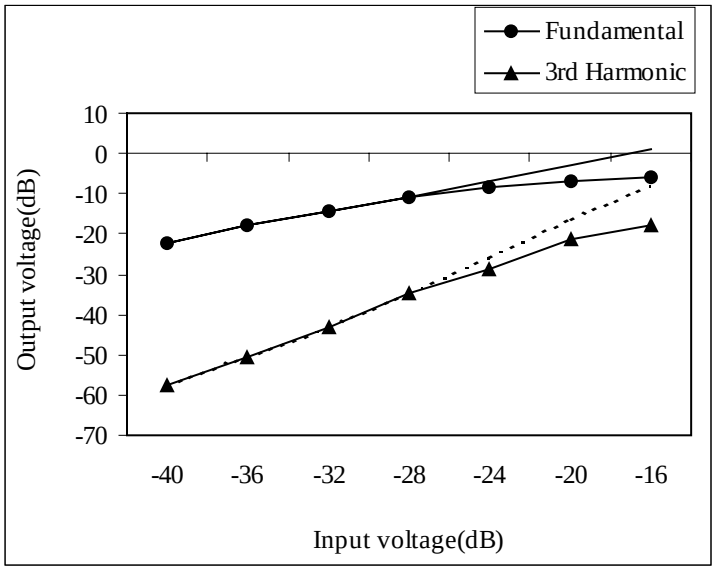

Fig.4.5 Results of IIP3 measurement

The results of the IIP3 test are shown in Fig.4.5. The straight-line overlapping the curve of the fundamental and the 3rd harmonic depicts the ideal case, that is, the absence of nonlinearity. But as the input voltage increases the amplifier enters a nonlinear region and the gain starts to drop from its ideal value. Both input and output voltages are expressed in terms of dB with a reference voltage of 1mV.

Doing transient analysis with varying input voltage and noting down where the gain of the amplifier drops by 1 dB gives the 1dB compression point of the amplifier.

4.2.3 Sensitivity analysis

Sensitivity analysis gives a measure of the sensitivity of the circuit performance to change in the circuit element values, i.e., it indicates which components affect performance most critically. This subsection describes sensitivity analysis of gain and noise figure to the inductors (L_G, L_S, L_D) as well as to different parameters of MOSFETs e.g., length, width and threshold voltages. The values of the inductors are varied over a range of $\pm$ 20 % whereas the MOS parameters (W, L, V_{TH} are varied over$\pm$5%). Relative change of gain and noise figure are plotted. The results are shown below:

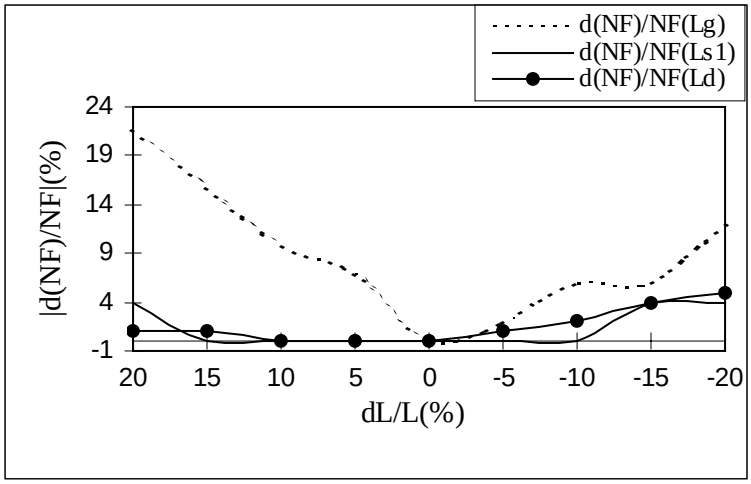

Fig.4.6 Variation of NF with variation in L_G, L_S, L_D

Noise figure is most sensitive to L_G as observed from Fig.4.6 whereas variation of L_S and L_D has negligible effect on noise figure.

Gain is most sensitive to L_D as one expects from the expression of gain given by $A_v=g_mZ_L$. It varies negligibly with L_S and L_D as observed from their corresponding curve that are closer to x-axis over most of the range.

Sensitivity analysis was also carried out by changing length of MOSFETs. But it was observed that neither gain nor noise figure varies significantly with change of length. So the results are excluded from this section.

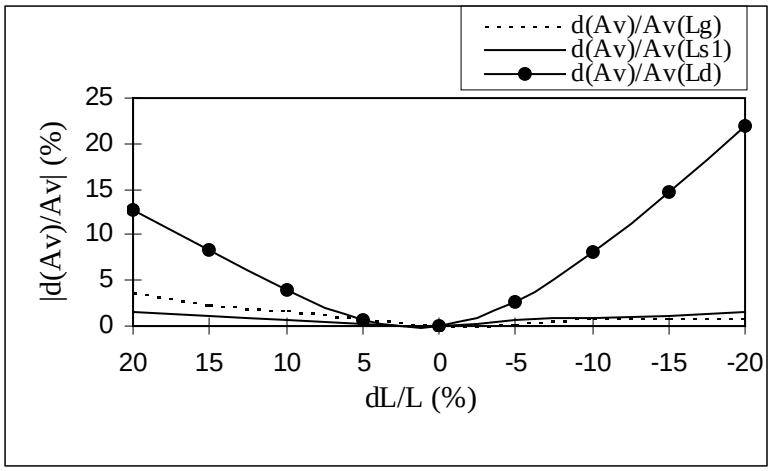

Fig.4.7. Variation of gain with variation in L_G, L_S, L_D

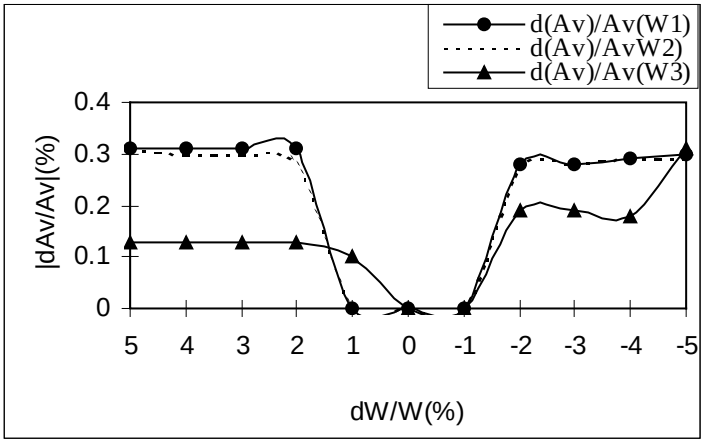

Fig.4.8. Variation of gain with variation in width of MOSFETs

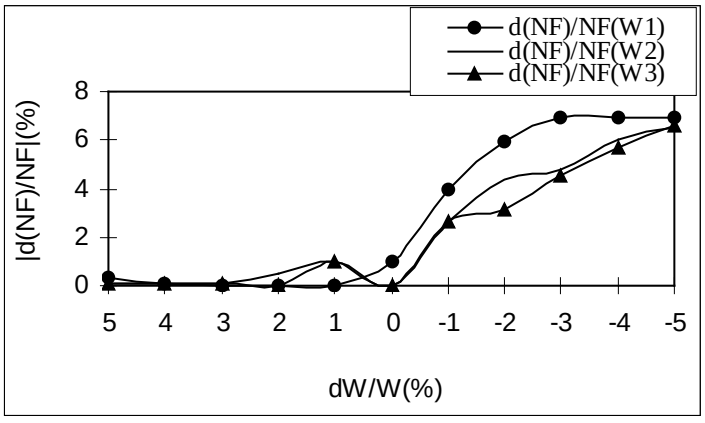

Fig.4.9. Variation of NF with variation in width of MOSFETs

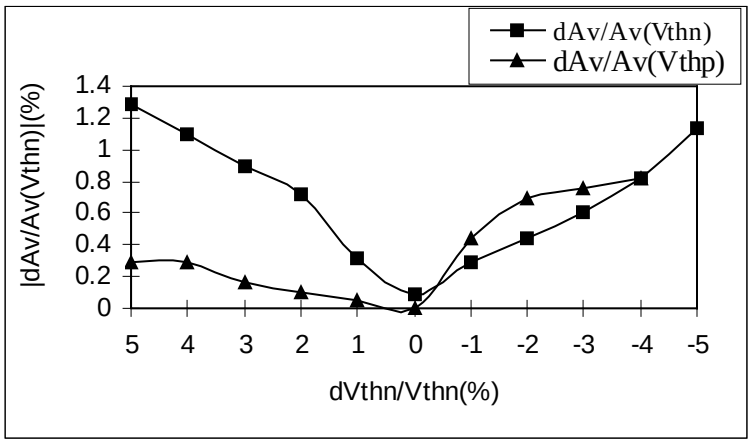

Fig.4.10. Variation of gain with change of V_{TH}

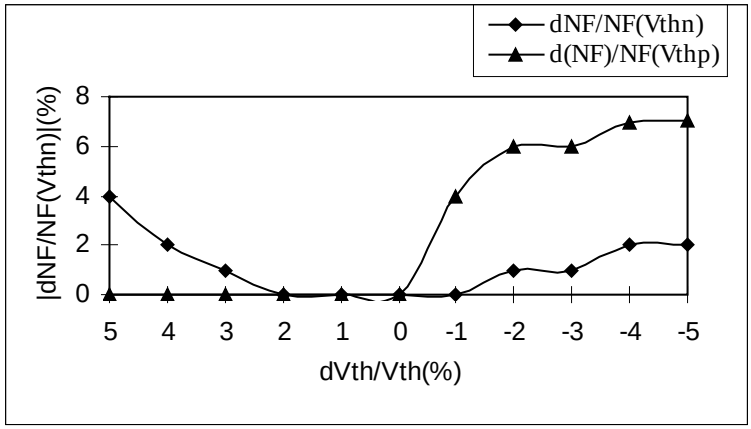

Fig.4.11. Variation of NF with change of V_{TH}

4.2.4 Comparison

Finally Table 4.1 compares various performance metrics of the different LNA.

As discussed in section 3.4.3 *folded cascode* architecture has a CS stage followed by a CG stage. This circuit consumes larger drain current to give comparable gain with that of inverter but power consumption of the circuit is lower as it works with a supply voltage of only 1V. The noise figure of the circuit is poor that the other configurations.

Degenerated current reuse architecture uses an inverter in place of the simple CS stage. The inverter provides higher gain than CS amplifier but this topology uses a resistor at the source of the CG amplifier. This reduces the gain of the inverter stage. Moreover this circuit works with V_{DD}=1.2V so if same amount of current flows to the CG stage as in the case of folded cascode the power consumption would be higher. To have comparable power consumption the drain current through CG amplifier is reduced which also reduces the gain of the overall circuit. It has almost same noise figure as that of folded cascode. This circuit has the drawback that, as an amplifier, its bias point is not stable, and a small change in its bias point makes either the PMOS or the NMOS to go out of saturation.

Table.4.1. Comparison of performances of different LNA topologies

Topology	Gain (dB)	NF (dB)	V_{DD} (V)	P_D (mW)	CP_{-1dB} (dBm)	IIP3 (dBm)
Folded Cascode	29.6	1.67	1.0	3.37	-14.01	-4.52
Degenerated Current Reuse LNA	29.24	1.60	1.2	3.62	-15.05	-6.48
Proposed LNA	32.01	1.0	1.2	3.50	-14.43	-5.92
Proposed LNA	29.17	1.38	1.1	2.00	-14.67	-6.00

The last two rows of the Table 4.1 give the performance of the proposed architecture with supply voltage of 1.2 V and 1.1 V respectively. This architecture uses a modified inverter followed by CG amplifier as shown in Fig.3.12. As PMOS and NMOS of the inverter are connected to different bias paths, their bias currents add up, which increases power consumption. The CG amplifier in this architecture has no source impedance, which implies greater gain. For this reason the proposed architecture when simulated with V_{DD}=1.2V, fails to achieve reduce power consumption but it gives a very good noise figure. For the second case, with V_{DD}=1.1V, the noise figure and gain degrade at the cost of reduced power consumption. This circuit has the added advantage that it stabilizes the drain voltage of the inverter.

Chapter 5

Conclusion and Future work

5.1 Summary

The design issues of CMOS LNAs are discussed and a novel LNA architecture is proposed. Simulation results, on a 0.18 μm MOS technology, show that for 2.4GHz LNA applications, compared to other existing architectures, the proposed architecture gives a lower noise figure, while giving comparable gain, power dissipation, and IIP3.

5.2 Future Scope

Future work can be carried in multiple directions. We are listing some of these here.

a) Sub-micron noise effects: Presently the noise in sub-micron MOSFETs is not well understood. A possible further direction of study is the modelling of noise. Though we have used the industry standard BSIM3v3.2.4 Spice model, the accuracy of this model at RF frequencies is questionable. This model accounts for drain noise but neglects the induced gate noise. Due to this effect, the exact noise response is expected to be even worse in real. The BSIM4 model would have been a better choice, but BSIM4 model parameters for state-of-the-art MOS technologies are not easily available.
b) Simulation of S-parameters: With the simulation tools available, S-parameters of the circuit could not be simulated. The circuit may be re-simulated using Cadence's Spectre-RF or Agilent's ADS.
c) Layout of the design: The layout of the proposed architecture was not done.

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Appendix A

BSIM3 Noise equivalent circuit

During the noise analysis, the SPICE simulator shorts out all independent voltage sources and opens up all the independent current sources. Each element is replaced by the element itself along with the noise sources, typically noise current, because adding a branch noise current is easier. Adding noise voltage implies creating an extra node in the circuit, which requires more computation time. Before doing a noise analysis SPICE finds DC bias point for the circuit and then performs an ac analysis with noise sources added in the circuit. The total noise voltage at a given node is equal to the sum of the noises contributed from all noise sources.
In case of MOSFET, BSIM3 considers the noise due to thermal noise of the channel current, flicker noise and thermal noise associated with the terminal source and drain resistance.

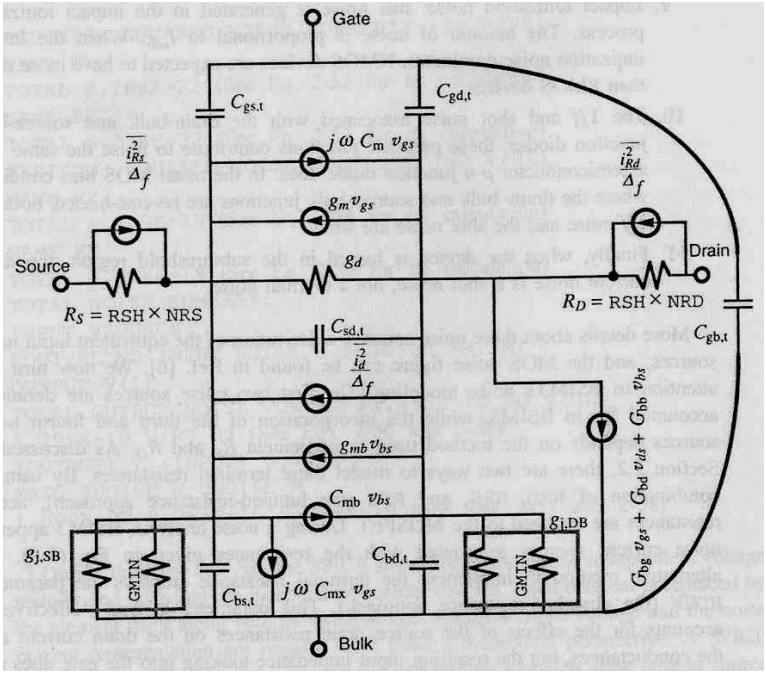

Fig.A.1.BSIM3 noise equivalent circuit [14]

Fig.A.1 shows the BSIM3 noise equivalent circuit whose high level representation is provided in Fig.A.2. Noise due to channel current and flicker noise is lumped into a single noise current source, the drain current ($i_d^2/\Delta f$) flowing in the intrinsic device.
BSIM3 considers the parasitic junction diodes to be noise free as the diodes are reverse biased for normal operation. Therefore no noise sources are associated with $g_{j,DB}$ and $g_{j,SB}$, which are the small signal conductance of the junction diodes. The resistor GMIN is added only for numerical convergence purpose. It does not represent any physical process.

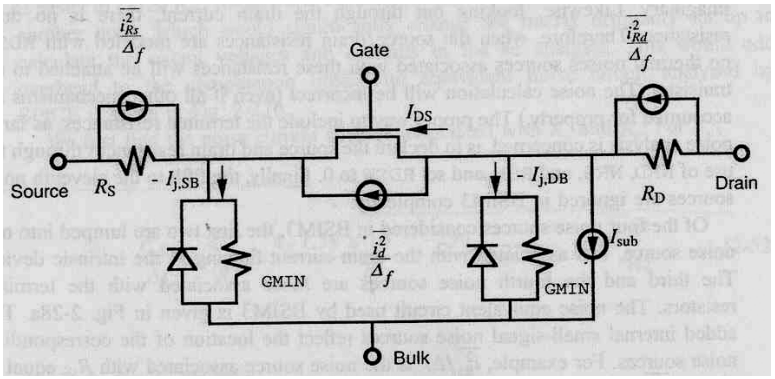

Fig.A.2.High level representation of BSIM3
noise equivalent circuit [14]

As the gate leakage current is almost negligible so BSIM3 does not consider the noise associated with it. Noise sources due to gate resistance and substrate resistance is also excluded since BSIM3 does not include these resistances in the model.

Appendix B

Measuring IP_n With Spice

The following gives the detail procedure on how to measure IIP3 with circuit simulator such as LTSpice.[20]

1. Apply two input signals by adding voltage sources in series with same amplitude (=30mV) but differing in frequency (in our simulation they are 2.4 GHz and 2.41GHz) though being in same band.
2. A transient analysis is done, for a time span of 1 μs. A sufficient time must pass so that at least ten cycles of the difference frequency (in this case, 10 MHz) is displayed. LTSpice displays output voltage amplitude vs. time, by default.

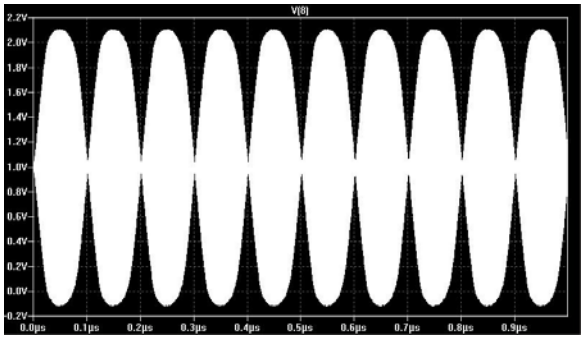

Fig.B.1.Transient response in LTSpice when two signals of different frequencies are applied

3. On this same display screen, select “FFT” to display output as a spectrum analyzer would.

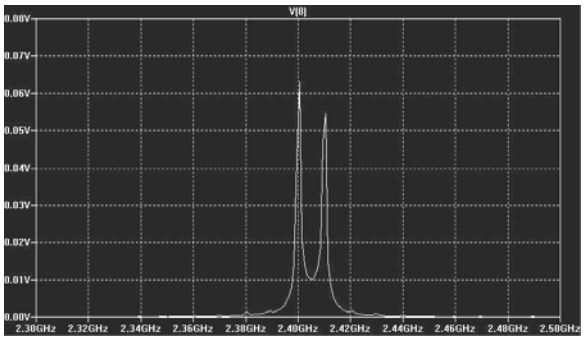

Fig.B.2. Result of IIP3 test in frequency domain with smaller input voltage

4. Choose a linear vertical display, and set horizontal span from 2.3 MHz. to 2.5 MHz. Only two signals show above this noise, with no distortion products visible.
5. Let's run this simulation again, with higher amplitudes at V1 and at V2 – say 100 mV each, pushing the amplifier to exhibit a little distortion. Now the IP3 distortion products appear above the noise floor, although they're still much smaller than the desired signals.

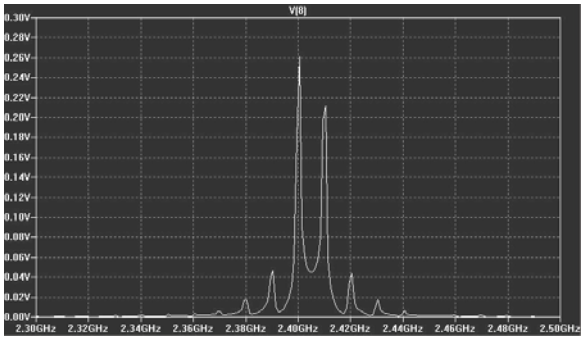

Fig.B.3.Result of IIP3 test in frequency domain
with larger input voltage

The values from the above measurement give the value of IIP3. For better accuracy the results where intermodulation are prominent are used for calculation of IIP3.

$$\text{Intermodulation Dynamic Range} = 2x(IP3_{out} – P_{out})$$

Intermodulation Dynamic Range is the ratio of desired signal to undesired signal. Let's in second case the desired output was –13.0 dBm, and undesired output was –58.0 dBm. The ratio here is 45. dB. Let Pin in the input power which equals to -21.0 dBm.So power gain of the amplifier is 8dB. Rearranging to find 3rd-order intercept at the output, IP3out,

$$IP3out = (IMDR + 2xP_{out}) / 2$$
$$=9.5 \text{ dBm}$$

The input intercept IP3in would be lower by a factor equal to amplifier gain

$$IP3in= IIP3=9.5-8.0=1.5 \text{ dBm}$$

Appendix C

Spice Model Parameters

```
.MODEL CMOSN NMOS (                       LEVEL   = 49
+VERSION = 3.1          TNOM    = 27          TOX     = 4.5E-9
+XJ      = 1E-7         NCH     = 2.3549E17   VTH0    = 0.3009266
+K1      = 0.4719837    K2      = -2.269515E-3  K3    = 1E-3
+K3B     = 6.1890183    W0      = 1E-7        NLX     = 2.09265E-7
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 0.453576     DVT1    = 0.5304762   DVT2    = -0.3024701
+U0      = 255.6677119  UA      = -1.792207E-9  UB    = 3.045963E-18
+UC      = 4.775695E-11  VSAT   = 1.229084E5   A0     = 2
+AGS     = 0.4151441    B0      = 3.390861E-7  B1     = 5E-6
+KETA    = -0.0151749   A1      = 0           A2      = 0.7050699
+RDSW    = 129.1545864  PRWG    = 0.5         PRWB    = -0.2
+WR      = 1            WINT    = 5.770178E-10  LINT   = 8.668955E-9
+DWG     = 3.516158E-9  DWB     = 2.13388E-8  VOFF    = -0.0815013
+NFACTOR = 1.8827224    CIT     = 0           CDSC    = 2.4E-4
+CDSCD   = 0            CDSCB   = 0           ETA0    = 1.855188E-3
+ETAB    = -1.741146E-6  DSUB   = 5.061009E-3  PCLM    = 1.2073617
+PDIBLC1 = 0.5110646    PDIBLC2 = 0.01        PDIBLCB = -0.1
+DROUT   = 0.8954571    PSCBE1  = 6.270848E9  PSCBE2  = 5.005E-10
+PVAG    = 0.1753703    DELTA   = 0.01        RSH     = 6.5
+MOBMOD  = 1            PRT     = 0           UTE     = -1.5
+KT1     = -0.11        KT1L    = 0           KT2     = 0.022
+UA1     = 4.31E-9      UB1     = -7.61E-18   UC1     = -5.6E-11
+AT      = 3.3E4        WL      = 0           WLN     = 1
+WW      = 0            WWN     = 1           WWL     = 0
+LL      = 0            LLN     = 1           LW      = 0
+LWN     = 1            LWL     = 0           CAPMOD  = 2
+XPART   = 0.5          CGDO    = 4.88E-10    CGSO    = 4.88E-10
+CGBO    = 1E-12        CJ      = 8.129808E-4  PB     = 0.8
+MJ      = 0.5210389    CJSW    = 1.868709E-10  PBSW   = 0.8
+MJSW    = 0.3616821    CJSWG   = 3.3E-10     PBSWG   = 0.8
+MJSWG   = 0.3616821    CF      = 0           PVTH0   = -5.110899E-4
+PRDSW   = -5           PK2     = 4.691964E-4  WKETA   = 3.629669E-4
+LKETA   = -2.984232E-4  PU0    = 13.1544464  PUA     = 6.753949E-11
+PUB     = 0            PVSAT   = 1.851358E3  PETA0   = -8.020553E-5
+PKETA   = 2.610545E-4  )

.MODEL CMOSP PMOS (                       LEVEL   = 49
+VERSION = 3.1          TNOM    = 27          TOX     = 4.5E-9
+XJ      = 1E-7         NCH     = 4.1589E17   VTH0    = -0.3972183
+K1      = 0.6164618    K2      = 2.455633E-3  K3     = 0
```

+K3B = 20 W0 = 1.00001E-6 NLX = 3.216589E-8
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 1.5721556 DVT1 = 1 DVT2 = -0.3
+U0 = 101.2240281 UA = 9.090542E-10 UB = 1.03579E-21
+UC = -1E-10 VSAT = 1.797274E5 A0 = 1.5153166
+AGS = 0.368943 B0 = 1.259527E-6 B1 = 2.992776E-6
+KETA = 0.0278143 A1 = 0.5501154 A2 = 0.3
+RDSW = 548.6092214 PRWG = 0.3087885 PRWB = -0.180581
+WR = 1 WINT = 0 LINT = 2.684789E-8
+DWG = -2.489387E-8 DWB = -9.950623E-9 VOFF = -0.1066497
+NFACTOR = 1.5029878 CIT = 0 CDSC = 2.4E-4
+CDSCD = 0 CDSCB = 0 ETA0 = 2.79939E-4
+ETAB = -1.280826E-3 DSUB = 0 PCLM = 2.3903966
+PDIBLC1 = 5.017244E-4 PDIBLC2 = 6.220185E-3 PDIBLCB = 0.1
+DROUT = 0 PSCBE1 = 5.765569E9 PSCBE2 = 1.730266E-9
+PVAG = 0 DELTA = 0.01 RSH = 6.2
+MOBMOD = 1 PRT = 0 UTE = -1.5
+KT1 = -0.11 KT1L = 0 KT2 = 0.022
+UA1 = 4.31E-9 UB1 = -7.61E-18 UC1 = -5.6E-11
+AT = 3.3E4 WL = 0 WLN = 1
+WW = 0 WWN = 1 WWL = 0
+LL = 0 LLN = 1 LW = 0
+LWN = 1 LWL = 0 CAPMOD = 2
+XPART = 0.5 CGDO = 4.34E-10 CGSO = 4.34E-10
+CGBO = 1E-12 CJ = 1.165977E-3 PB = 0.8214639
+MJ = 0.4256548 CJSW = 1.220056E-10 PBSW = 0.8
+MJSW = 0.1 CJSWG = 4.22E-10 PBSWG = 0.8
+MJSWG = 0.1 CF = 0 PVTH0 = -5.259015E-5
+PRDSW = -0.0788372 PK2 = 3.77628E-4 WKETA = 0.0498907
+LKETA = -0.0143262 PU0 = -0.1732571 PUA = 5.027662E-12
+PUB = 1.136171E-22 PVSAT = 49.8423845 PETA0 = 1.003159E-4
+PKETA = -5.597782E-3)